Bumblebee (LBB-1)
Whiskeylake-U Schematics

Project Code: 4PD0G1010001
PCB(Raw Card): 18729-1

2019-05-30

Properties of DUMMY: (BOM Control Parts)

Value	Description
(No Value)	ASM, assemble
DY	DUMMY, NOT ASM, not assemble
ZZ (No Need to Display)	ZZ parts for testpoint / shortpad / hole
PCBID	PCB ID for SW Team (PCB number)
SKUID	SKU ID for SW Team (CPU Type: non-vPro / vPro)
MEM_IDx_0 / MEM_IDx_1 (x = 0~4)	Memory ID for SW Team (0 = Low / 1 = High Level)
DDR4_CTRL	Memory Packaging Technology setting (SDP / DDP)
SDP / DDP	Number of identical die in package (1 = SDP, 2 = DDP)
APS / ISH / LPC / XDP	Debug Connectors (Assemble in 1st build only)
EMC	Follow EMC Team requested
NON_PSL / PSL	Support / Non Support KBC Power Switched Logic
WLAN_PCIe / WLAN_CNVi	Support WLAN type (PCIe or CNVi interface)
CHARGER_HS / CHARGER_LS	Charger High / Low Side MOSFET
VCCSA_HS / VCCSA_LS	VCCSA High / Low Side MOSFET

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: COVER PAGE

Size	Document Number	Rev
A4	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 1 of 99

Bumblebee-1 Whiskeylake Block Diagram

Project Code: 4PD0G1010001
PCB(Raw Card): 18729-1

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating	Size
10KR3	10K Ohm	If no letter, it means J: 5%	0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DESCRIPTION

BOM control parts :
TEXT with PURPLE color near part reference

BOM control name
Part reference
Symbol name

PCB Layer Stackup

L1:Component
L2:GND
L3:Signal 1
L4:VCC
L5:Signal 2
L6:Signal 3
L7:GND
L8:Signal 4
L9:GND
L10:Component

Battery Charger/Selector BQ25700ARSNR 44
VINT20_IN | 19V_DCBATOUT BT+

System DC/DC TPS51285B 45
19V_DCBATOUT | 5V_S5 3D3V_S5

DC/DC IMVP8 NCP81218MNTXG 46

DC/DC VCCCPUCORE NCP302045LMNTXG 47
19V_DCBATOUT | 1V_CPU_CORE

DC/DC VCCGT NCP302045LMNTXG 48
19V_DCBATOUT | 1V_VCCGT

DC/DC VCCSA NCP81253MNTBG 50
19V_DCBATOUT | 1V_VCCSA

DC/DC 1D2V_S3 NB687GQ-C669-Z 51
19V_DCBATOUT | 1D2V_S3

DC/DC 0D6V_VREF_S0 NB687GQ-C669-Z 51
1D2V_S3 | 0D6V_VREF_S0

DC/DC 2D5V_S3 NB687GQ-C669-Z 51
3D3V_S5 | 2D5V_S3

DC/DC 1D05V_SUS RT8237CZQW 52
19V_DCBATOUT | 1D05V_SUS

DC/DC 1D8V_SUS RT5797ALGQW 53
3D3V_S5 | 1D8V_SUS

Touch Panel 55 — Port 6 — USB 2.0 480Mb/s
LCD 13.3" FHD/HD 55 — eDP 1.3 (2 Lanes)
HDMI 1.4b 57 — DP/HDMI Mux PS8337B 56 — DDI 5.4GT/s
DP/USB Mux PS8747 58 — Port 2 USB3.1
USB TYPE-C USB1 75
USB TYPE-C (CS18 Docking) DK1 74 — Thunderbolt Alpine Ridge 71 — DDI 5.4GT/s
25MHz (X7101)

DDR4-Memory Down 1 12
DDR4-Memory Down 2 13
DDR4*2 2400MT/s

Wireless LAN Antenna
WLAN on board Jefferson Peak M.2 1216 Bluetooth 61
USB 2.0 Port 10 (BT)

Wireless WAN Antenna
WWAN 62 — Type B M.2 3042 — Micro SIM Slot 63
USB 2.0 Port 7 (WWAN)

Smart Card Reader 94 — Port 1 — USB2.0 x10 Ports
USB TYPE-C USB1 75 — Port 2 — USB3.0 x4 Ports
USB TYPE-A (AOU) USB3 36 — Port 3
USB TYPE-A USB4 36 — Port 4
USB TYPE-C (CS18 Docking) DK1 74 — Port 5
Touch Panel 55 — Port 6
M.2 WWAN Slot 62 — Port 7
RBG Camera / IR Camera DMIC Module 66 — Port 8
FingerPrint (Optional) 92 — Port 9
Bluetooth CNVi WLAN's BT 61 — Port 10
Reserved — Port 1
Port 2
USB TYPE-A (AOU) GEN1 USB3 36 — Port 3
USB TYPE-A GEN1 USB4 36 — Port 4
RTC Battery 25
Active Pen 93 — Power (3.3V)
Power Button 64 — KBC_PWRBTN#

CPU
Intel Whiskeylake-U Series
vPro/Non-vPro
ISH | ME | Clock Generator
PCH-LP 4~11, 15~23

I2C (PCH_I2C0)
SM Bus_3B
I2C (ISH_I2C0)
SPI
C-Link 66MHz(Vpro only)
PCI Express x4 Ports
SATA 6Gb/s x1
IHDA

SPI Flash 32MB 25
TPM 2.0 91
24MHz (X1801)
PECI 3.0
LPC Bus 24MHz
32.768KHz (X1802)

Port 13 (1x) (Gen 2) (WLAN)
Port 15 (1x) (Gen 2) (WWAN)
Port 9 (4x) (Gen 3) (SSD)
Port 14 (1x) (Gen 2) (GbE)
Port 1 (1x) (Gen 2) (Card)

Type M M.2 2280-S3 SSD 63

GbE PHY Intel 219LM/V 31
25MHz (X3101)
Card Reader RTS5232S-GR 33
Micro SD Slot 33

G-Sensor Angle Calculate Control LIS2DH12TR 70 — I2C (ISH_I2C0)
G-Sensor Thermal Control LIS2DWLTR 70 — I2C
NFC (Optional) 90 — I2C
KBC_PWRBTN#

Embedded Controller NPCE388 24

HDA CODEC Realtek ALC3287-CG 27
Internal Mic
DMIC Module 66
Stereo Speaker 29
HP/MIC
30 Audio Jack (Microphone /Headphone)

SM Bus_3B
SMBus
Thermal Sensor NCT7717U+NCT7718W 26
ClickPad 65
Keyboard/Backlight TrackPoint 65
FAN 26

USB Type-C Adapter
Battery Charger 44
SMB Bus
Main Battery 43
DC/DC Converter 45
RTC Battery 25
3D3V_AUX_S5

External Connector/Socket
Internal Connector/Socket
Internal Switch

LBB-1
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21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: BLOCK DIAGRAM
Size: A2 | Document Number: Bumblebee-1 | Rev: -1
Date: Thursday, May 30, 2019 | Sheet 2 of 99

Main Func = CPU

BB1_EVT_MAIN_W015
BB1_SVT_MAIN_W008

24 PECI_CPU
24,44,46 PROCHOT#_CPU

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

1D05V_VCCSTG
1D05V_VCCST
Rb R301 1KR2J-1-GP
R329 49D9R2F-GP
Ra
PROCHOT#_CPU
THERMTRIP#_EC
R302 1 2 499R2F-2-GP
R328 1 2 0R2-PT5-LILY-GP-U
THERMTRIP#_CPU
TPAD14-OP-GP TP304
TPAD14-OP-GP TP305
TPAD14-OP-GP TP302
TPAD14-OP-GP TP303
BPM_CPU_N0 U1
BPM_CPU_N1 U2
BPM_CPU_N2 U3
BPM_CPU_N3 U4
-TBT_PLUG_EVENT
R319 1 2 0R2J-2-GP
R320 1 2 0R2J-2-GP
R304 2 1 49D9R2F-GP
R305 2 1 49D9R2F-GP
GPP_E3 CE9
CN3
CB34
GPP_B3 CC35
GPP_B4
CPU_POPIRCOMP BP27
PCH_POPIRCOMP BW25

CPU1D 4 OF 20
CATERR# AA4
PECI AR1
PROCHOT# Y4
THRMTRIP# BJ1
BPM#0
BPM#1
BPM#2
BPM#3
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
PROC_POPIRCOMP
PCH_OPIRCOMP
PROC_TCK T6
PROC_TDI U6
PROC_TDO Y5
PROC_TMS T5
PROC_TRST# AB6
PCH_TCK W6
PCH_TDI U5
PCH_TDO W5
PCH_TMS P5
PCH_TRST# Y6
PCH_JTAGX P6
PROC_PREQ# W2
PROC_PRDY# W1
WHISKEY-LAKE-GP

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

1D05V_VCCST
R308 1KR2J-1-GP
THERMTRIP#_CPU

1D05V_VCCSTG
PROC_TDO R321 1 100R2J-2-GP

If PCH_TDO is set to Termination, R321 is 100ohm.
If PROC_TDO uesd, R321 is 51ohm.

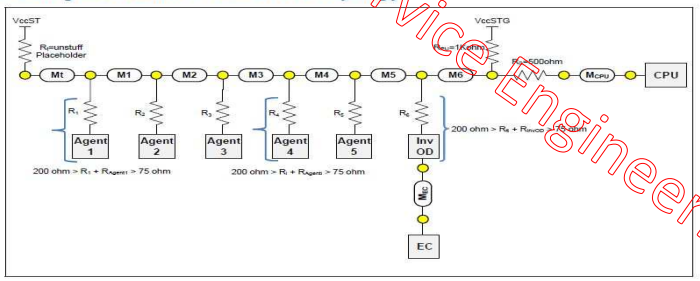
PROC_TCK R322 1 51R2J-2-GP
PCH_JTAG_TCK R326 1 51R2J-2-GP
DY

71 -TBT_PLUG_EVENT

99 PROC_TCK
99 PROC_TDI
99 PROC_TMS
99 PROC_TRST#
99 PCH_JTAG_TCK
99 PROC_TDO
99 PROC_PREQ#
99 PROC_PRDY#
40 THERMTRIP#_EC

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

LBB-1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (THML/JTAG)
Size: A3
Document Number: Bumblebee-1
Rev: -1
Date: Thursday, May 30, 2019
Sheet 3 of 99

Main Func = CPU

BB1_EVT_MAIN_W008
BB1_EVT_MAIN_W024
BB1_SIT_MAIN_W026

DOCK

71 DP1_DDI_TX_N0
71 DP1_DDI_TX_P0
71 DP1_DDI_TX_N1
71 DP1_DDI_TX_P1
71 DP1_DDI_TX_N2
71 DP1_DDI_TX_P2
71 DP1_DDI_TX_N3
71 DP1_DDI_TX_P3
71 DP1_AUX_CPU_N
71 DP1_AUX_CPU_P
71 DP1_HPD_CPU

USBC

56 DP2_DDI_TX_N0
56 DP2_DDI_TX_P0
56 DP2_DDI_TX_N1
56 DP2_DDI_TX_P1
56 DP2_DDI_TX_N2
56 DP2_DDI_TX_P2
56 DP2_DDI_TX_N3
56 DP2_DDI_TX_P3
56 DP2_AUX_CPU_N
56 DP2_AUX_CPU_P
56 DP2_HPD_CPU

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 eDP_HPD_CPU

24 L_BKLT_EN
55 L_BKLT_CTRL
55 EDP_VDD_EN

15 GPP_H17_STRAP

24 EC_SM#

56 DP2_SCL_CPU
56 DP2_SDA_CPU

62 WWAN_PERST#

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

CHECK WHL design guide: DISP_RCOMP

1D05V_VCCIO
R401 24D9R2F-L-GP
eDP_RCOMP_CPU → AM6 DISP_RCOMP

3D3V_SUS
R407 2K2R2J-2-GP DP1_SDA_CPU
3D3V_SUS
RN402 SRN2K2J-1-GP DP2_SDA_CPU DP2_SCL_CPU
R404 10KR2J-3-GP EC_SM#

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

TABLE: Functional Strap

DDPB_CTRLDATA **HIGH Port B is detected.** **LOW Port B is not detected.**
DDPC_CTRLDATA **HIGH Port C is detected.** **LOW Port C is not detected.**

SOC: DDI2, DDI1
DEMUX PS8337B: DP, TMDS
SWITCH PS8747B
USB TYPE-C
HDMI CONN
For TBT Display

CPU1A — 1 OF 20 — WHISKEY-LAKE-GP

DP1_DDI_TX_N0	AL5	DDI1_TXN0	
DP1_DDI_TX_P0	AL6	DDI1_TXP0	
DP1_DDI_TX_N1	AJ5	DDI1_TXN1	
DP1_DDI_TX_P1	AJ6	DDI1_TXP1	
DP1_DDI_TX_N2	AF6	DDI1_TXN2	
DP1_DDI_TX_P2	AF5	DDI1_TXP2	
DP1_DDI_TX_N3	AE5	DDI1_TXN3	
DP1_DDI_TX_P3	AE6	DDI1_TXP3	
DP2_DDI_TX_N0	AC4	DDI2_TXN0	
DP2_DDI_TX_P0	AC3	DDI2_TXP0	
DP2_DDI_TX_N1	AC1	DDI2_TXN1	
DP2_DDI_TX_P1	AC2	DDI2_TXP1	
DP2_DDI_TX_N2	AE4	DDI2_TXN2	
DP2_DDI_TX_P2	AE3	DDI2_TXP2	
DP2_DDI_TX_N3	AE1	DDI2_TXN3	
DP2_DDI_TX_P3	AE2	DDI2_TXP3	
		DDI1_AUX_N	
		DDI1_AUX_P	
		DDI2_AUX_N	
		DDI2_AUX_P	
		DDI3_AUX_N	
		DDI3_AUX_P	
	AG4	EDP_TXN0	eDP_TX_CPU_N0
	AG3	EDP_TXP0	eDP_TX_CPU_P0
	AG2	EDP_TXN1	eDP_TX_CPU_N1
	AG1	EDP_TXP1	eDP_TX_CPU_P1
	AJ4	EDP_TXN2	
	AJ3	EDP_TXP2	
	AJ2	EDP_TXN3	
	AJ1	EDP_TXP3	
	AH4	EDP_AUX_N	eDP_AUX_CPU_N
	AH3	EDP_AUX_P	eDP_AUX_CPU_P
	AM7	EDP_DISP_UTILS	TP401 TPAD14-OP-GP
	AC7	DISP_UTILS	DP1_AUX_CPU_N
	AC6		DP1_AUX_CPU_P
	AD4		DP2_AUX_CPU_N
	AD3		DP2_AUX_CPU_P
	AG7		
	AG6		
	CN6	GPP_E13/DDPB_HPD0/DISP_MISC0	DP1_HPD_CPU
	CM6	GPP_E14/DDPC_HPD1/DISP_MISC1	DP2_HPD_CPU
	CP7	GPP_E15/DDPD_HPD2/DISP_MISC2	WWAN_PERST#
	CP6	GPP_E16/DDPE_HPD3/DISP_MISC3	EC_SMI#
	CM7	GPP_E17/EDP_HPD/DISP_MISC4	EDP_HPD_CPU
	CK11	EDP_BKLTEN	L_BKLT_EN
	CG11	EDP_VDDEN	EDP_VDD_EN
	CH11	EDP_BKLTCTL	L_BKLT_CTRL
	CP4	GPP_E22/DDPD_CTRLCLK	
	CN4	GPP_E23/DDPD_CTRLDATA	
	CR26	GPP_H16/DDPF_CTRLCLK	
	CP26	GPP_H17/DDPF_CTRLDATA	
	CC8	GPP_E18/DDPB_CTRLCLK/CNV_BT_HOST_WAKE#	
	CC9	GPP_E19/DDPB_CTRLDATA	
	CH4	GPP_E20/DDPC_CTRLCLK	
	CH3	GPP_E21/DDPC_CTRLDATA	

TPAD14-OP-GP TP402 — GPP_E23_STRAP — reserved for strap

R403 100KR2J-1-GP
R402 100KR2J-1-GP
R406 100KR2J-1-GP
R405 100KR2J-1-GP

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

LBB-1

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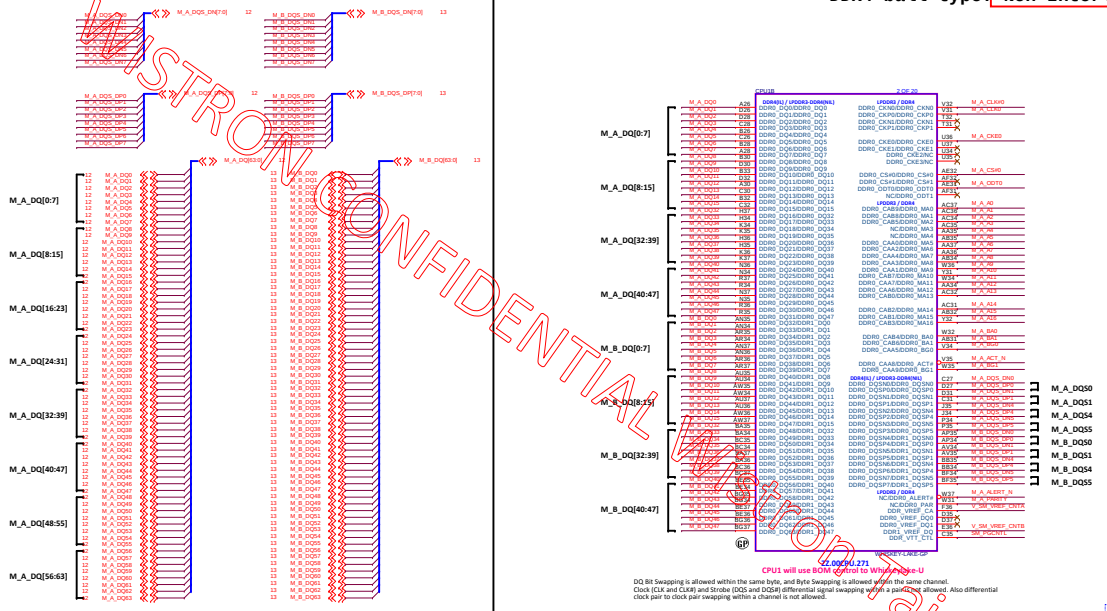
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

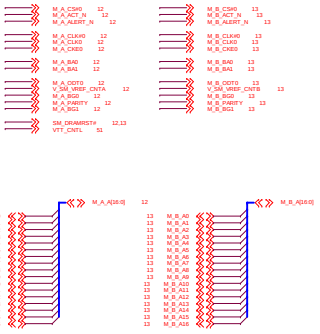
Title: CPU (DDI/EDP)
Size: A2 | Document Number: Bumblebee-1 | Rev: -1
Date: Thursday, May 30, 2019 | Sheet 4 of 99

Main Func = CPU

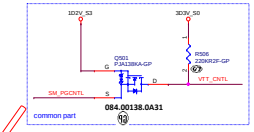
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W040
BB1_EVT_MAIN_W017

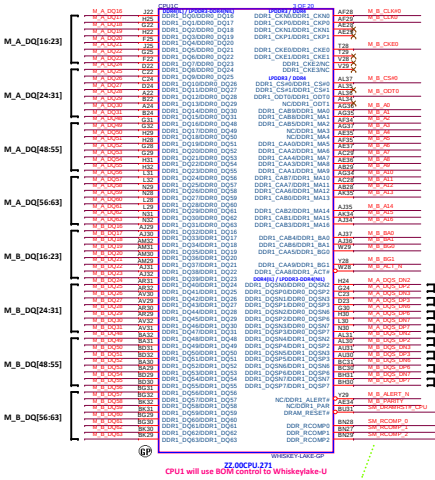
DDR4 ball type: Non-Interleaved Type

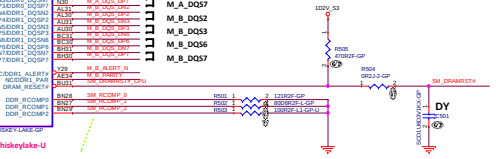




DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping with a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.







Layout Note:

#575412 Rev 1.5
Table 4-8. WHL-U/CFL-U DDR4 x16 Memory Down Routing Guideline (mils)

Design Guideline:
SM_RCOMP_0/1/2 keep routing length less than 500 mils.

#575412 Rev 1.5
Table 4-8. WHL-U/CFL-U DDR4 x16 Memory Down Routing Guideline (mils)

DDR - DDR4 X 16 Memory Down
DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS
DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS
DDR_RCOMP[2]: 100Ω ±1% on pkg to VSS

LBB-1

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU(CFG/IST)		
Size: A1	Document Number: Bumblebee-1	Rev: -1
Date: Thursday, May 30, 2019	Sheet 5 of 89	

Main Func = CPU

PCH strap pin: CFG3 CFG4

ZZ.00CPU.271

CPU1 will use BOM control to Whiskeylake-U

LBB-1

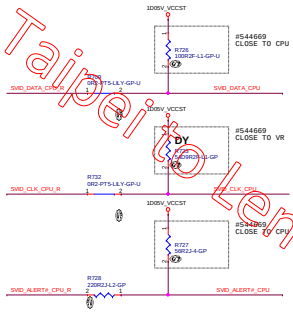
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU(CFG/IST)		
Size: A2	Document Number: Bumblebee-1	Rev: -1
Date: Thursday, May 30, 2019	Sheet 6 of 99	

Layout Note:
The total length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID DATA

SVID CLOCK

SVID ALERT



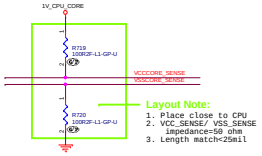


Figure 10-7. Routing Illustration for SVID Topology

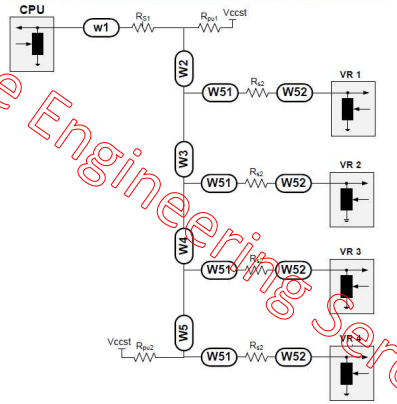


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PAU} [Ω]	R_{PAD} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCCpr [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

Title: CPU(VCC_CORE)
Size: A1 | Document Number: Bumblebee-1 | Rev: -1
Date: Thursday, May 30, 2019 | Sheet 7 of 55

Main Func = CPU

BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W017
BB1_SIT_MAIN_W014

46 VCCGT_SENSE
46 VSSGT_SENSE
46 VSSSA_SENSE
46 VCCSA_SENSE

1V_VCCGT
CPU1M
13 OF 20
WHL QS/CFL/WHL_ES1_CNL U
1V_CPU_CORE
WHISKEY-LAKE-GP
ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

1D2V_S3
DY
C804
SC1U6D3V1MX-GP

1V_VCCIO (ICCMAX.=2.73A
1D05V_VCCIO
CPU1N
14 OF 20
1V_VCCSA
RSVD#BC28
WHISKEY-LAKE-GP
ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

1D05V_VCCST
0.04 A
C801
SC1U6D3V1MX-GP

1D05V_VCCSTG
C802
SC1U6D3V1MX-GP

1D2V_VCCSFR_OC
C803
SC1U6D3V1MX-GP

1D05V_VCCST
0.12 A
C807
C808
C805
C806
SC22U6D3V2MX-GP-U
SC1U6D3V1MX-GP
SC01U6D3V1KX-GP

WHL VCCPLL Power CAPs:
Intel PDG recommended
1 x 22uF/47uF 0805
=> L86-1 layout impact:
2 x 22uF 0402

1V_VCCGT
R807
100R2F-L1-GP-U
R808
100R2F-L1-GP-U
VCCGT_SENSE
VSSGT_SENSE

1V_VCCSA
R810
100R2F-L1-GP-U
R809
100R2F-L1-GP-U
VCCSA_SENSE
VSSSA_SENSE

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(VDDQ/VCC/VCCSTI/VCCSTG)
Size: A2
Document Number: Bumblebee-1
Rev: -1
Date: Thursday, May 30, 2019
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LBB-1

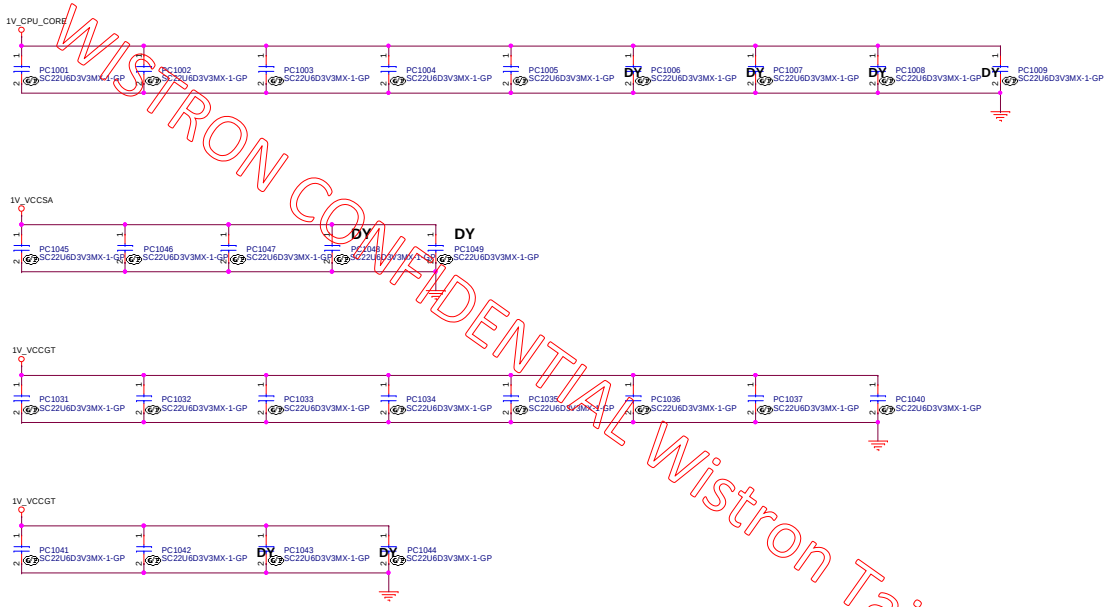
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

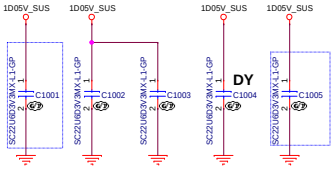
Title: CPU (RSVD)

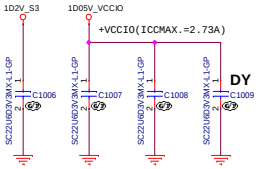
Size	Document Number	Rev
A4	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 9 of 99

Main Func = CPU





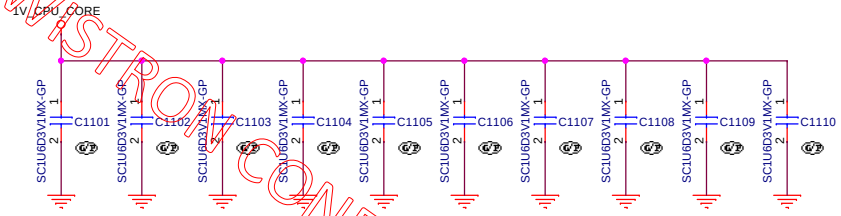


LBB-1

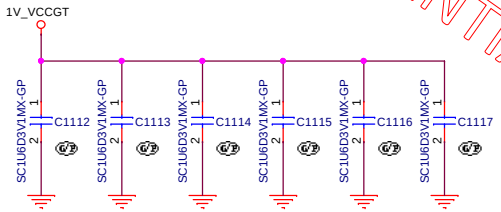
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (POWER CAP1)		
Size: A2	Document Number: Bumblebee-1	Rev: -1
Date: Thursday, May 30, 2019	Sheet 10 of 99	

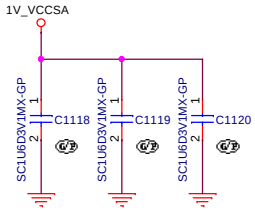
VCORE WHL U42

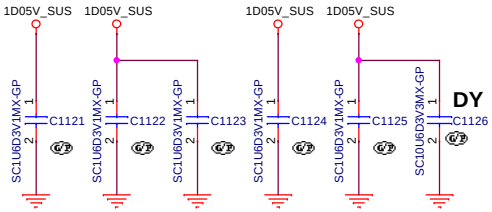


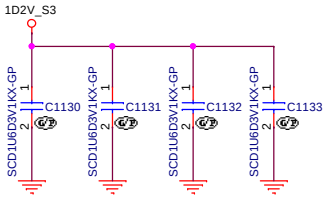
VCCGT WHL U42

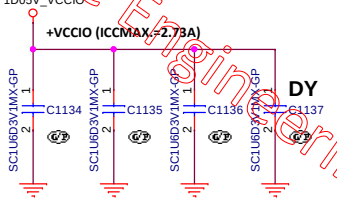


VCCSA WHL U42









LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

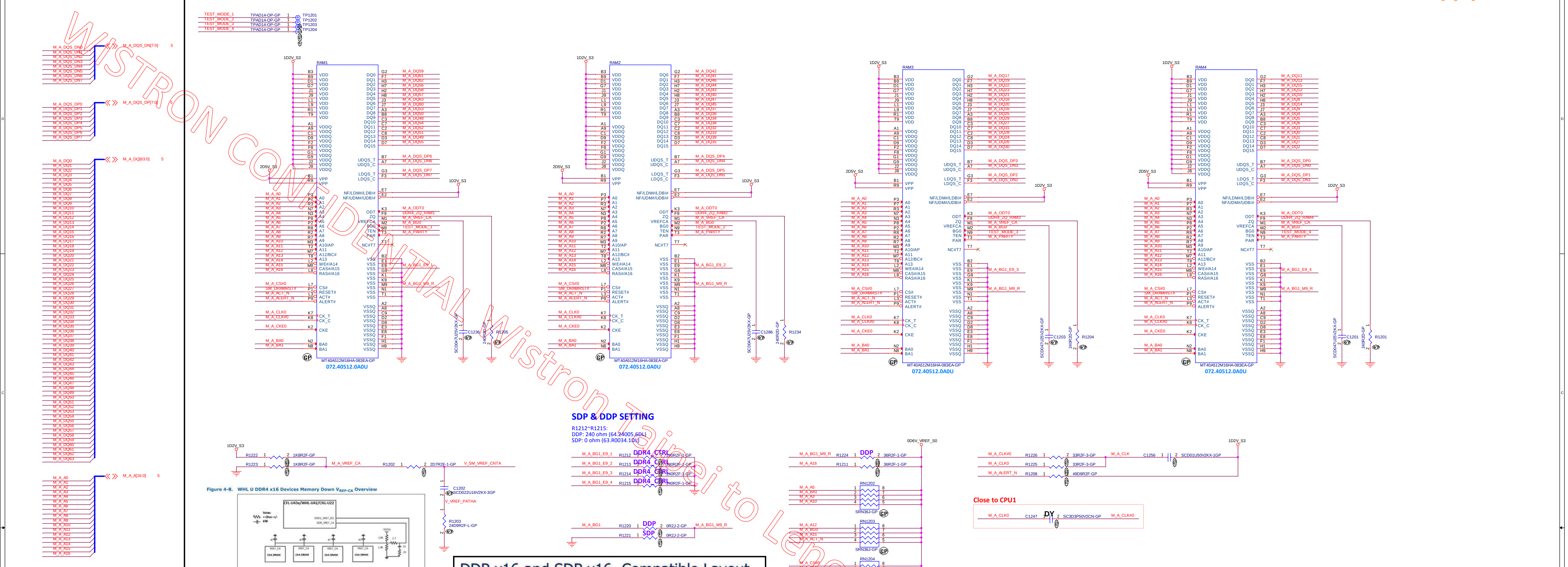
Title: CPU (POWER CAP2)

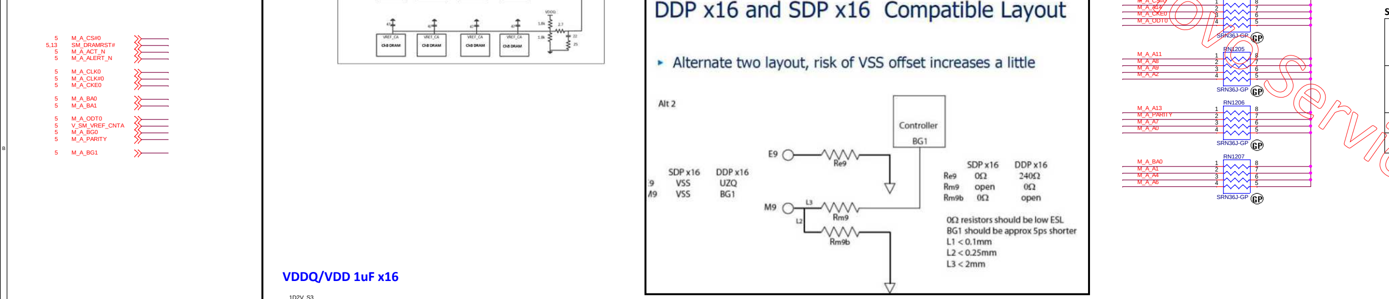
Size: A3 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 11 of 99

Main Func = DIMM1

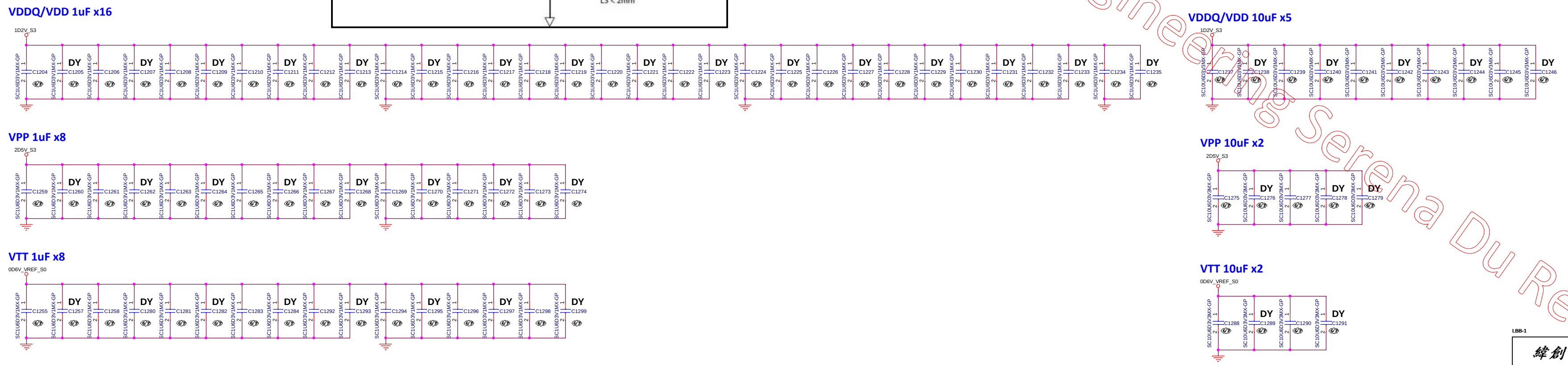
BB1_EVT_MAIN_W009
BB1_EVT_MAIN_W031
BB1_EVT_MAIN_W044





SDP and DDP BOM Control Table

		SDPx16 8Gb			DDPx16 16Gb		
		SM30N76502AA Samsung K4A8G165WC-BCTD	SM30N76518AA SK Hynix H5AN8G6NCJR-VKC	SM30N76490AA Micron MT40A512M16LY-075:E	SM30N76504AA Samsung K4AAG165WB-MCTD	SM30N07785AA SK Hynix H5ANAG6NAMR-VKC	SM30E51324AA Micron MT40A1G16KNR-075:E
DDR4_CTRL	R1212 R1213 R1214 R1215	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	240R 1% 240R 1% 240R 1% 240R 1%	240R 1% 240R 1% 240R 1% 240R 1%	240R 1% 240R 1% 240R 1% 240R 1%
SDP	R1221	ASM	ASM	ASM	DY	DY	DY
DDP	R1220 R1224	DY DY	DY DY	DY DY	ASM ASM	ASM ASM	ASM ASM



LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHA)

Size: A1 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 12 of 99

BB1_EVT_MAIN_W099
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W044

SDP & DDP SETTING

R1331*R1334:
DDP: 240 ohm (64.5+300/5.6Ω)
SDP: 0 ohm (63.R0034.1I0)

DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little

Alt 2

	SDP x16	DDP x16
9	VSS	UZQ
A9	VSS	BG1

	SDP x16	DDP x16
Re9	0Ω	240Ω
Rm9	open	0Ω
Rm9b	0Ω	open

0Ω resistors should be low ESL
BG1 should be approx 5ps shorter
L1 < 0.1mm
L2 < 0.25mm
L3 < 2mm

Close to CPU1

SDP and DDP BOM Control Table

		SDPx16 8Gb			DDPx16 16Gb		
		SM30N76502AA Samsung K4A8G165WC-BCTD	SM30N76518AA SK Hynix H5AN8G6NCJR-VKC	SM30N76490AA Micron MT40A512M16LY-075:E	SM30N76504AA Samsung K4AAG165WB-MCTD	SM30N0778SAA SK Hynix H5ANAG6NAMR-VKC	SM30ES1324AA Micron MT40A1G16KNR-075:E
DDR4_CTRL	R1331	0R	0R	0R	240R 1%	240R 1%	240R 1%
	R1332	0R	0R	0R	240R 1%	240R 1%	240R 1%
	R1333	0R	0R	0R	240R 1%	240R 1%	240R 1%
	R1334	0R	0R	0R	240R 1%	240R 1%	240R 1%
SDP	R1340	ASM	ASM	ASM	DY	DY	DY
DDP	R1339	DY	DY	DY	ASM	ASM	ASM
	R1312	DY	DY	DY	ASM	ASM	ASM

VDDQ/VDD 1uF x16

VDDQ/VDD 10uF x5

VPP 1uF x8

VPP 10uF x2

VTT 1uF x8

VTT 10uF x2

Wistron Corporation	5F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: DDR (DDR4-CHB)	
Size: A1	Document Number: Bumblebee-1
Rev: -1	
Date: Thursday, May 30, 2019	Sheet 13 of 38

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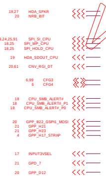
LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (RSVD)		
Size: A4	Document Number: Bumblebee-1	Rev: -1
Date: Thursday, May 30, 2019	Sheet 14 of 99	

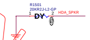
Main Func = PCH

HW Strap



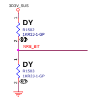
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). *Notes:* 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

GPP_B14



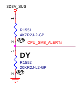
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_B18



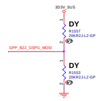
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_C2



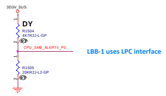
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). Bit 6 — Boot BIOS Destination 0 — SPI (Default) 1 — LPC *Notes:* 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

GPP_B22



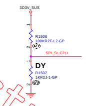
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning:** If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)

GPP_C5



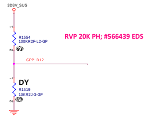
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_MOSI



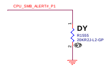
GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_D12



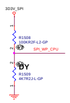
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.

GPP_B23



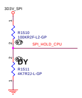
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2



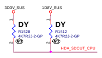
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3



HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_R2 / HDA_SDO / I2S0_TXD / HDACPU_SDO



GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. **Notes:** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

on page 71

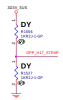
GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. **Notes:** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

on page 4

GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

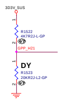
RO13_CFLU_20180130 follow RO13 to GPP_E23 strap (remove R1528)

GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



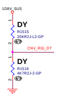
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on PCH strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_H21

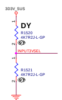


GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

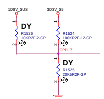
GPP_F6 / CNV_RGI_DT / UART0_TXD



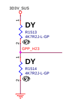
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% **Note:** This strap should only be used for specific targeted 1S battery systems.



GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling



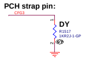
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning:** This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)



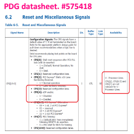
[DDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)

CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

PCH strap pin:



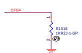
PDG datasheet. #575418



(#543016)

DISPLAY PORT PRESENCE STRAP

CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.



Main Func = PCH

TBT AR-LP

M.2 PCIe SSD

WLAN

GbE PHY

WWAN

Media Card Reader

USB3.1 Type-C X-bar switch (PS8747)

USB TYPE-A (AOU) GEN1 / USB3

USB TYPE-A GEN1 / USB4

Smart Card Reader

USB TYPE-C / USB1

USB TYPE-A (AOU) / USB3

USB TYPE-A / USB4

USB TYPE-C (CS18 Docking) / DK1

Touch Panel

M.2 WWAN Slot

RGB Camera & IR Camera

Fingerprint

CPU1H

8 OF 20

ZZ_00CPU-271
CPU1 will use BOM control to Whiskeylake-U

Support CNVi

CNVi Bluetooth

Intel Checklist #575179 Note:
Support CNVi WLAN's Bluetooth: Please connect to CPU USB2N/P_10 (WHLU)

Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

(#571021_CFLU) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

SATA Configuration	
Pair	Device
0	NC
1A	M.2 SATA SSD
1B	NC
2	NC

PCIe Configuration	
Pair	Device
1	Media Card Reader
2	NC
3	NC
4	NC
5	TBT (AR-LP)
6	TBT (AR-LP)
7	NC
8	NC
9	M.2 PCIe SSD
10	M.2 PCIe SSD
11	M.2 PCIe SSD
12	M.2 PCIe SSD
13	WLAN
14	GbE
15	NC
16	WWAN

USB3.0 Configuration	
Pair	Device
1	NC
2	USB3 Type-C Port1
3	USB3 Type-A Port3 (AOU)
4	USB3 Type-A Port4
5	NC
6	NC

USB2.0 Configuration	
Pair	Device
1	Smart Card Reader
2	USB3 Type-C Port1
3	USB3 Type-A Port3 (AOU)
4	USB3 Type-A Port4
5	USB3 Type-C (CS18 Docking) Port2 / DK1
6	Touch Screen
7	WWAN Card
8	RGB/IR Hybrid Camera
9	Fingerprint
10	Bluetooth (CNVi)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size	Document Number	Rev
A1	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 16 of 89

Main Func = PCH

BB1_EVT_MAIN_W006
BB1_EVT_MAIN_W015
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W037
BB1_EVT_MAIN_W040
BB1_EVT_MAIN_W042
BB1_FVT_MAIN_W013
BB1_FVT_MAIN_W017
BB1_FVT_MAIN_W034
BB1_SIT_MAIN_W008
BB1_SIT_MAIN_L006

#575412, v0.9, p.30: 1M-ohm PU and 330K-ohm is used on the CRB

PDG #575412 p128

BATLOW#:
Pull-up required even if not implemented.

AOZ Power Switch P/N: 074.01334.0093
Low Rds(on): 5mΩ(typ)
Turn on rise time = 10us

Dis-wire with XDP_PM_RSMRST_PWRGD_XDP

Follow wistron ORS design.

22.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

LCASE BTN2

R1715 PD for CNVI

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

Wistron Corporation	5F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: PCH (PMU)	
Size: A1	Document Number: Bumblebee-1
Rev: -1	
Date: Thursday, May 30, 2019	Sheet 17 of 89

Main Func = PCH

BB1_EVT_MAIN_W006
BB1_EVT_MAIN_W015
BB1_EVT_MAIN_W024
BB1_EVT_MAIN_W020
BB1_EVT_MAIN_W021
BB1_EVT_MAIN_W032
BB1_SVT_MAIN_W008

PCH strap pin: SPI_SO_CPU

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PCH strap pin: CPU_SMB_ALERT#_P0

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.

Media Card Reader
TBT
M.2 PCIe SSD
WWAN
GbE PHY
WLAN

PH on WWAN Conn

Close CPU1

R1843: LPC Debug Port for Security (Page 68)

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

24MHz (X1801)
TXC 7V24000023 082.30006.0571
HARMONY X3G024000BC1HA-HU 082.30006.0531

32.768KHz (X1802)
EPSON EP.FC-135R 32.768K12.5+-20 (X1A000141000300) 082.30003.0191
SEIKO Q.SC32P03220C5AAAF 082.30003.0301
TXC 9H03200042 082.30003.0231

Wistron Corporation	
Title: CPU_(SPI/ESPI/SMBUS/XTAL/CLK)	
Size: A1	Document Number: Bumblebee-1
Rev: -1	
Date: Thursday, May 30, 2019	Sheet 18 of 89

Main Func = PCH

BB1_SIT_MAIN_W015 BB1_EVT_MAIN_L020
BB1_SIT_MAIN_W028 BB1_EVT_MAIN_L009
BB1_SVT_MAIN_W002 BB1_SIT_MAIN_L002
BB1_SVT_MAIN_W008

PCH strap pin: HDA_SDOUT_CPU

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

SW Control :

GPP_G1	
SD_MMC_ID	Low = REALTEK [RTS5232S]
	High = GENESYS [GL9750]

HW Control : *

R1903	R1904
1M-ohm	1K-ohm
1K-ohm	1M-ohm

<-- Default

27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC
15 HDA_SDOUT_CNV
25 RTC_TEST

24 ME_FWP_EC

61 CLKREQ0_CNVI
61 RF_RESET_B_CNVI

15,27 HDA_SPKR

61 BLUETOOTH_EN_CPU

71 TBT_RTD3_PWR_EN
71 TBT_FORCE_USB_PWR
71 -TBT_PERST
71 -TBT_PCIE_WAKE

24 TOP_SWAP_EN

62 WWAN_ANTENNA#

CPU1G 7 OF 20

HDA_SYNC_CPU	BN34	HDA_SYNC/I2S0_SFRM	GPP_G0/SD_CMD	CH36	BLUETOOTH_EN_CPU
HDA_BITCLK_CPU	BN37	HDA_BCLK/I2S0_SCLK	GPP_G1/SD_DATA0	CL35	SD_MMC_ID
HDA_SDOUT_CPU	BN36	HDA_SDO/I2S0_TXD /strap	GPP_G2/SD_DATA1	CL36	RTC_TEST
HDA_SDIN0_CPU	BN35	HDA_SDI0/I2S0_RXD	GPP_G3/SD_DATA2	CM35	
	BL36	HDA_SDI1/I2S1_RXD/SNDW1_DATA	GPP_G4/SD_DATA3	CN35	TBT_RTD3_PWR_EN
HDA_RST_N_CPU	BL35	HDA_RST#/I2S1_SCLK/SNDW1_CLK	GPP_G5/SD_CD#	CH35	TBT_FORCE_USB_PWR
	CK23	GPP_D23/I2S_MCLK	GPP_G6/SD_CLK	CK36	-TBT_PERST
	BL37	I2S1_SFRM/SNDW2_CLK	GPP_G7/SD_WP	CK34	-TBT_PCIE_WAKE
	BL34	I2S1_TXD/SNDW2_DATA			
RF_RESET_B_CNVI	CJ32	GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#			
CLKREQ0_CNVI	CH32	GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK			
GPP_H1_SFRM	CH29	GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ			
GPP_H2_CLKREQ0	CH30	GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO			
	CP24	GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7		BW36	WWAN_ANTENNA_CPU
TOP_SWAP_EN	CN24	GPP_D19/DMIC_CLK0/SNDW4_CLK	GPP_A16/SD_1P8_SEL	BY33	
		GPP_D20/DMIC_DATA0/SNDW4_DATA			
	CK25		SD_1P8_RCOMP	CK33	SD_RCOMP
	CJ25	GPP_D17/DMIC_CLK1/SNDW3_CLK	SD_3P3_RCOMP	CM34	
		GPP_D18/DMIC_DATA1/SNDW3_DATA			
HDA_SPKR	CF35	GPP_B14/SPKR /strap			

WHISKEY-LAKE-GP

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

3D3V_SUS

TPAD14-OP-GP TP1903 1 HDA_RST_N_CPU

R1903 1 SDID 2 1MR2J-1-GP
R1904 1 SDID 2 1KR2J-1-GP

RF_RESET_B_CNVI R1913 1 2 33R2J-2-GP GPP_H1_SFRM
CLKREQ0_CNVI R1912 1 2 33R2J-2-GP GPP_H2_CLKREQ0
TOP_SWAP_EN R1902 1 2 0R2-PT5-LILY-GP-U

WWAN_ANTENNA#
DY
Q1901 LSK3541G1ET2L-GP
WWAN_ANTENNA_CPU G D S
SD_RCOMP R1901 1 2 200R2F-L-GP

PCH strap pin: SPKR

TOP SWAP OVERRIDE	
HDA_SPKR	* High = TOP SWAP ENABLED Low = DISABLED (WEAK INTERNAL PD)

The internal pull-up

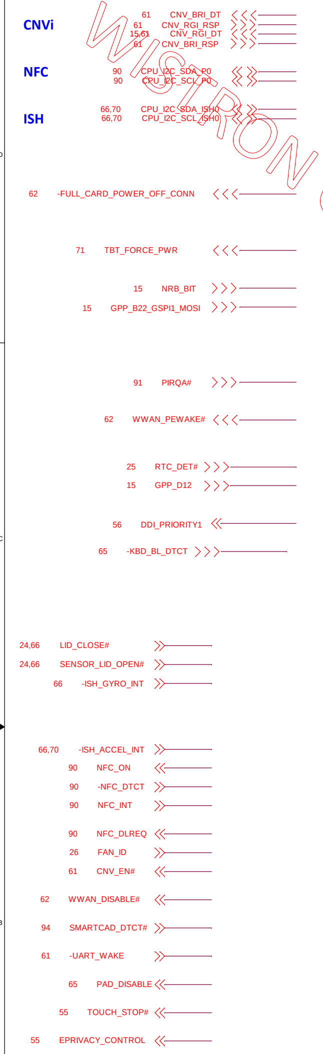
HDA_SYNC_CODEC R1908 1 2 33R2J-2-GP HDA_SYNC_CPU
HDA_BITCLK_CODEC R1920 1 2 33R2J-2-GP HDA_BITCLK_CPU
HDA_SDOUT_CODEC R1921 1 2 33R2J-2-GP HDA_SDOUT_CPU
ME_FWP_EC R1909 1 2 1KR2J-1-GP
R1914 1 DY 2 10KR2J-3-GP TOP_SWAP_EN

LBB-1

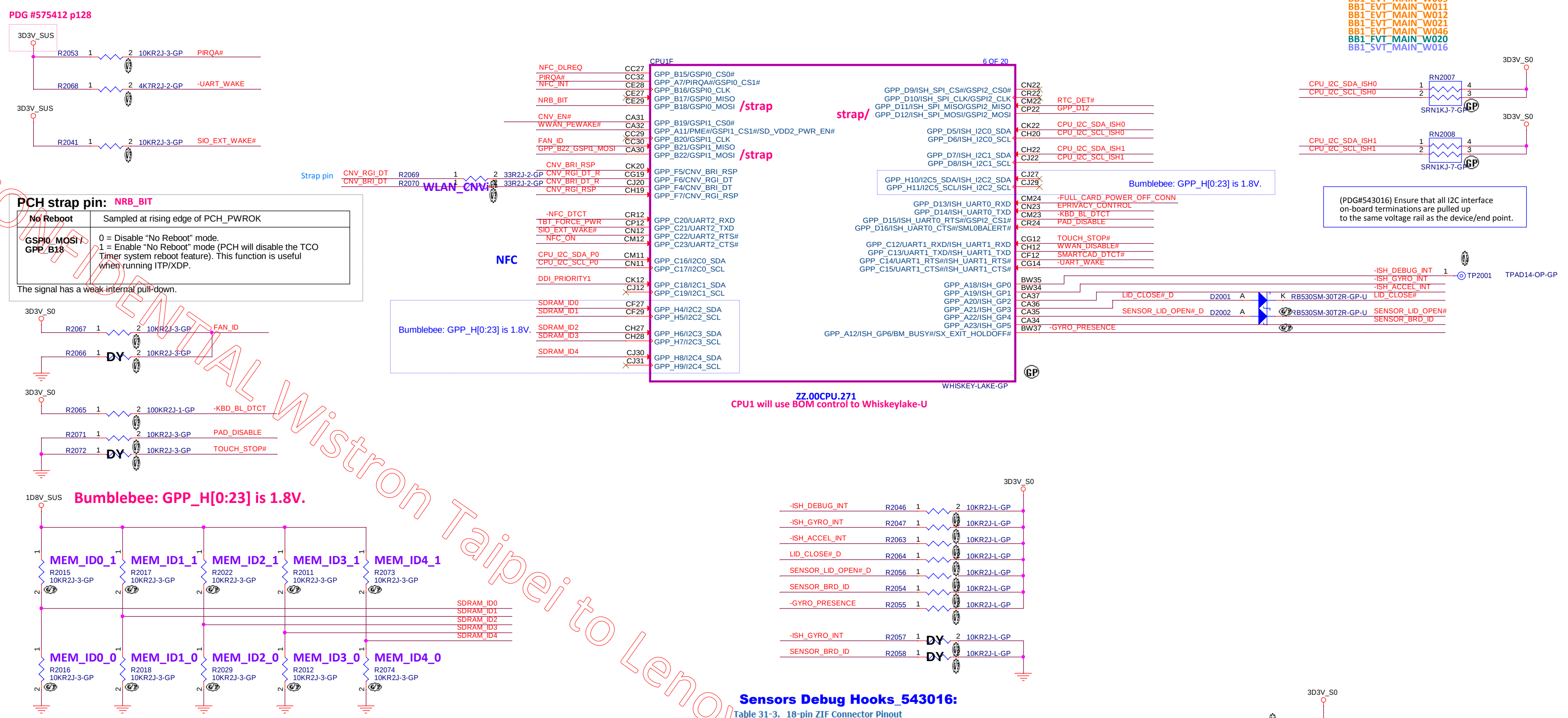
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(HDA/I2S/SD/DMIC)
Size: A2 | Document Number: Bumblebee-1 | Rev: -1
Date: Thursday, May 30, 2019 | Sheet 19 of 99

BB1_EVT_MAIN_W008
BB1_EVT_MAIN_W009
BB1_EVT_MAIN_W011
BB1_EVT_MAIN_W012
BB1_EVT_MAIN_W021
BB1_EVT_MAIN_W046
BB1_FVT_MAIN_W020
BB1_SVT_MAIN_W016
BB1_FVT_MAIN_L002



PDG #575412 p128



PCH strap pin: NRB_BIT

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

EVT/FVT/SIT/SVT:

Memory Configuration	Memory Supplier	Die Revision
00: 8Gb 01: 4Gb (Reserve) 10: 16Gb 11: 32Gb (Reserve)	00: Samsung 01: Micron 10: SK Hynix 11: (Reserve)	

GPP_H8	GPP_H7	GPP_H6	GPP_H5	GPP_H4				
SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Memory ID	Supplier	Density	Vendor PN
0	0	0	0	0	0	SAMSUNG	8GB (8Gb*8)	K4A8G165WC-BCTD
~~0~~	~~1~~	~~0~~	~~0~~	~~0~~	~~8~~			
1	0	0	0	0	16	SAMSUNG	16GB (16Gb*8)	K4AAG165WB-MCTD
~~1~~	~~1~~	~~0~~	~~0~~	~~0~~	~~24~~			
0	0	0	1	0	2	MICRON	8GB (8Gb*8)	MT40A512M16LY-075:E
0	0	0	1	1	3	MICRON	8GB (8Gb*8)	MT40A512M16TB-062E:J
1	0	0	1	0	18	MICRON	16GB (16Gb*8)	MT40A1G16KNR-075:E
~~1~~	~~1~~	~~0~~	~~1~~	~~0~~	~~26~~			
0	0	1	0	0	4	SK HYNIX	8GB (8Gb*8)	H5AN8G6NCJR-VKC
~~0~~	~~1~~	~~1~~	~~0~~	~~0~~	~~12~~			
1	0	1	0	0	20	SK HYNIX	16GB (16Gb*8)	H5ANAG6NAMR-UHC
1	0	1	0	1	21	SK HYNIX	16GB (16Gb*8)	H5ANAG6NCMR-VKC

0=L, 1=H

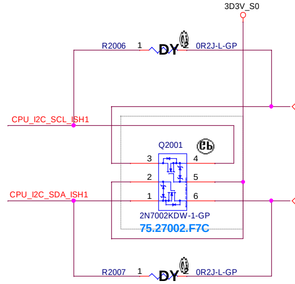
SOVP: (The Alternation of Memory Supplier SAMSUNG, MICRON and SK HYNIX)

SDRAM_ID4 R2073 R2074	SDRAM_ID3 R2011 R2012	SDRAM_ID2 R2022 R2029	SDRAM_ID1 R2017 R2018	SDRAM_ID0 R2015 R2016	Memory ID	Supplier	Density	Vendor PN
DY 10K	DY 10K	1.2M 1.2K	1.0M 1.0K	6.2M 6.2K	0	SAMSUNG	8GB (8Gb*8)	K4A8G165WC-BCTD
10K DY	DY 10K	1.2M 1.2K	1.0M 1.0K	6.2M 6.2K	16	SAMSUNG	16GB (16Gb*8)	K4AAG165WB-MCTD
DY 10K	DY 10K	2.2M 2.2K	2.0K 2.0M	8.2M 8.2K	2	MICRON	8GB (8Gb*8)	MT40A512M16LY-075:E
DY 10K	DY 10K	2.2M 2.2K	2.0K 2.0M	8.2K 8.2M	3	MICRON	8GB (8Gb*8)	MT40A512M16TB-062E:J
10K DY	DY 10K	2.2M 2.2K	2.0K 2.0M	8.2M 8.2K	18	MICRON	16GB (16Gb*8)	MT40A1G16KNR-075:E
DY 10K	DY 10K	4.3K 4.3M	2.7M 2.7K	10M 10K	4	SK HYNIX	8GB (8Gb*8)	H5AN8G6NCJR-VKC
10K DY	DY 10K	4.3K 4.3M	2.7M 2.7K	10M 10K	20	SK HYNIX	16GB (16Gb*8)	H5ANAG6NAMR-UHC
10K DY	DY 10K	4.3K 4.3M	2.7M 2.7K	10K 10M	21	SK HYNIX	16GB (16Gb*8)	H5ANAG6NCMR-VKC

Sensors Debug Hooks_543016:

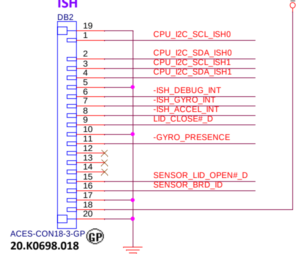
Table 31-3. 18-pin ZIF Connector Pinout

Pin	Pin function	Description
1	ISH_I2C0_SCL	Clock line for the I2C0
2	ISH_I2C0_SDA	Data line for the I2C0
3	ISH_I2C1_SCL	Clock line for the I2C1
4	ISH_I2C1_SDA	Data line for the I2C1
5	GND	System Ground
6	GPIOa (1)	Connect here one of the GPIOs in use
7	GPIOb (1)	Connect here one of the GPIOs in use
8	GPIOc (1)	Connect here one of the GPIOs in use
9	GPIOd (1)	Connect here one of the GPIOs in use
10	GND	System Ground
11	Reserved by Intel	Do not use
12	Reserved by Intel	Do not use
13	Reserved by Intel	Do not use
14	Reserved by Intel	Do not use
15	Reserved by Intel	Do not use
16	Reserved by Intel	Do not use
17	GND	System Ground
18	Vio	Sensors Reference Voltage



Sensors Debug Hooks

ISH



Main Func = PCH

BB1_EVT_MAIN_W009 BB1_SIT_MAIN_W002 BB1_SVT_MAIN_W008 BB1_EVT_MAIN_L001

CNVi

61 CNV_WT_DN0
61 CNV_WT_DP0
61 CNV_WT_DN1
61 CNV_WT_DP1
61 CNV_WT_CLK_DN
61 CNV_WT_CLK_DP
61 CNV_WR_DN0
61 CNV_WR_DP0
61 CNV_WR_DN1
61 CNV_WR_DP1
61 CNV_WR_CLK_DN
61 CNV_WR_CLK_DP
61 WIFI_RF_EN_CPU
68 CPU_UARTx_RXD
68 CPU_UARTx_TXD
40 CPU_C10_GATE#
15 GPP_H21
15 GPD_7
15 GPP_H23
62 -WWAN_RESET
62 WWAN_CFG0
62 WWAN_CFG1
62 WWAN_CFG2
62 WWAN_CFG3
65,90 NFC_ACTIVE
66 IR_CAM_DET#
66 DMIC_DET#
17 -TAMPER_SW_DTCT

CPU1I 9 OF 20

CNVi

CNV_WR_DN0 CR30 CNV_WR_D0N
CNV_WR_DP0 CP30 CNV_WR_D0P
CNV_WR_DN1 CM30 CNV_WR_D1N
CNV_WR_DP1 CN30 CNV_WR_D1P
CNV_WT_DN0 CN32 CNV_WT_D0N
CNV_WT_DP0 CM32 CNV_WT_D0P
CNV_WT_DN1 CP33 CNV_WT_D1N
CNV_WT_DP1 CN33 CNV_WT_D1P
CNV_WR_CLK_DN CN31 CNV_WR_CLKN
CNV_WR_CLK_DP CP31 CNV_WR_CLKP
CNV_WT_CLK_DN CP34 CNV_WT_CLKN
CNV_WT_CLK_DP CN34 CNV_WT_CLKP

R2101 2 1 150R2F-1-GP CNV_WT_RCOMP CP32 CNV_WT_RCOMP#CP32
CR32 CNV_WT_RCOMP#CR32
R2120 0R2J-2-GP DY
NFC_ACTIVE 1 2 WWAN_CFG2 CP20 GPP_F0/CNV_PA_BLANKING
-WWAN_RESET CK19 GPP_F1
NFC_ACTIVE_CPU CG17 GPP_F2

Debug Card

CPU_UARTx_RXD CR14 GPP_C8/UART0_RXD
CPU_UARTx_TXD CP14 GPP_C9/UART0_TXD
IR_CAM_DET# CN14 GPP_C10/UART0_RTS#
DMIC_DET# CM14 GPP_C11/UART0_CTS#
WWAN_CFG0 CJ17 GPP_F8/CNV_MFUART2_RXD
WWAN_CFG1 CH17 GPP_F9/CNV_MFUART2_TXD
GPP_F23 CF17 GPP_F23/A4WP_PRESENT

R2102 100KR1J-GP

3D3V_S0
R2122 1 10KR2J-3-GP IR_CAM_DET#
R2123 1 10KR2J-3-GP DMIC_DET#

GPP_H18/CPU_C10_GATE# CN27 GPPC_H18_BOOTMPC
GPP_H19/TIMESYNC0 CM27
GPP_H21 CF25 GPP_H21
GPP_H22 CN26
GPP_H23 CM26 GPP_H23
GPP_F10 CK17
GPD7 BV35 GPD_7
GPP_F3 CN20
GPP_D4/IMGCLKOUT0/BK4/SBK4 CG25 WIFI_RF_EN_CPU
GPP_H20/IMGCLKOUT1 CH25
GPP_F12/EMMC_DATA0 CR20
GPP_F13/EMMC_DATA1 CM20
GPP_F14/EMMC_DATA2 CN19
GPP_F15/EMMC_DATA3 CM19
GPP_F16/EMMC_DATA4 CN18
GPP_F17/EMMC_DATA5 CR18
GPP_F18/EMMC_DATA6 CP18
GPP_F19/EMMC_DATA7 CM18
GPP_F: VCCPGPPF = 1.8V Only
GPP_F20/EMMC_RCLK CM16
GPP_F21/EMMC_CLK CP16
GPP_F11/EMMC_CMD CR16 WWAN_CFG3
GPP_F22/EMMC_RESET# CN16 -TAMPER_SW_DTCT_CPU
EMMC_RCOMP CK15 EMMC_RCOMP

R2119 0R2J-2-GP DY 1 2 CPU_C10_GATE#
R2121 0R2-PT5-LILY-GP-U 1 2 -TAMPER_SW_DTCT
R2108 1 2 200R2F-L-GP

GP

WHISKEY-LAKE-GP

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(CSI/EMMC/CNVI)

Size: A3 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 21 of 99

Main Func = PCH

BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W016
BB1_EVT_MAIN_W017
BB1_EVT_MAIN_W020
BB1_SVT_MAIN_W008
BB1_EVT_MAIN_L007

CPU1P — 16 OF 20 — WHISKEY-LAKE-GP

VCCDSW_1P05 (BT24): PCH internal VRM

VCCRTCEXT (BP24): PCH internal VRM

VCCDPHY_1P24 (BY23 CA23 CP25 BY24 CA24): PCH internal VRM

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

C2224 close to BR24

R2206: For DEEP Sx leakage debug

CPU1O — 15 OF 20 — WHISKEY-LAKE-GP

ZZ.00CPU.271
CPU1 will use BOM control to Whiskeylake-U

TBD
Layout Note:
1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19

Layout Note:
C2208 near BV2
C2209 near BV2

Layout Note:
0.1uF:
C2225 near BT20

TBD
Layout Note:
22uF:
C2113 near K15

TBD
Layout Note:
1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1

Layout Note:
C2221 near BR23
C2222 near BR23

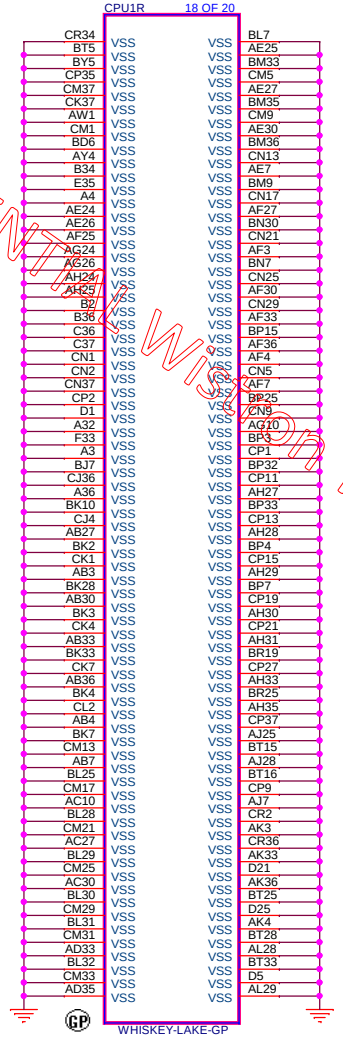
TBD
Layout Note:
1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

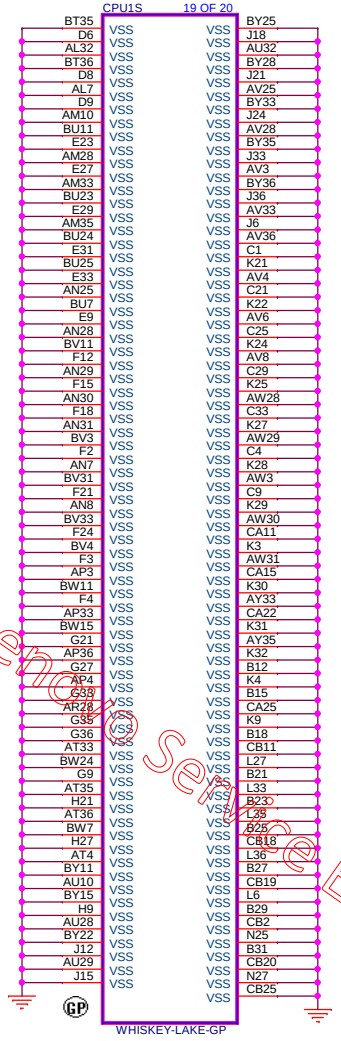
LBB-1

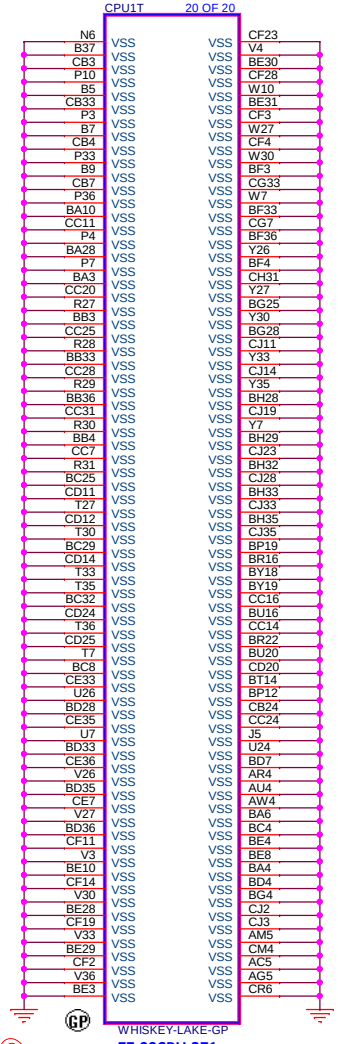
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(PCH-LP PWR&CAPS)
Size: A2
Document Number: Bumblebee-1
Rev: -1
Date: Thursday, May 30, 2019
Sheet 22 of 99

Main Func = PCH







LBB-1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)		
Size: A3	Document Number: Bumblebee-1	Rev: -1
Date: Thursday, May 30, 2019	Sheet 23 of 99	

Main Func = KBC

BB1_EVT_MAIN_W010
BB1_EVT_MAIN_W012
BB1_EVT_MAIN_W014
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W039
BB1_EVT_MAIN_W004
BB1_EVT_MAIN_W012
BB1_EVT_MAIN_W017
BB1_EVT_MAIN_W020
BB1_EVT_MAIN_W025
BB1_EVT_MAIN_W042
BB1_SIT_MAIN_W003
BB1_SIT_MAIN_W004
BB1_SIT_MAIN_W009
BB1_SIT_MAIN_W013
BB1_SIT_MAIN_W018
BB1_SIT_MAIN_W028
BB1_SIT_MAIN_W029
BB1_SVT_MAIN_W003
BB1_SVT_MAIN_W007
BB1_SVT_MAIN_W008
BB1_EVT_MAIN_L001
BB1_SIT_MAIN_L005

SKU_ID (PIN D4)		Pull Down (R2449)	Pull High (R2448)	Voltage
LBB-1	vPro	100.0K	10.0K	3V
	non-vPro		20.0K	2.75V
	vPro	100.0K	33.0K	2.481V
	non-vPro		47.0K	2.245V
	vPro	100.0K	64.9K	2.001V
	non-vPro		76.8K	1.867V
	vPro	100.0K	100.0K	1.650V
	non-vPro		143.0K	1.358V

← LOGIC

PCB_ID (PIN D1)	Pull Down (R2419)	Pull High (R2418)	Voltage
18729-SA	100.0K	10.0K	3V
18729-SB	100.0K	20.0K	2.75V
18729-SC	100.0K	33.0K	2.481V
18729-1	100.0K	47.0K	2.245V
	100.0K	64.9K	2.001V
	100.0K	76.8K	1.867V
	100.0K	100.0K	1.650V
	100.0K	143.0K	1.358V

← LOGIC

Nuvoton KBC NPCE388PB0BX

LPC or eSPI Strapping BIOS Function Selection:

LPC_ESPI_STRAP1 (Pin U2401.N1)	LPC_ESPI_STRAP0 (Pin U2401.J6)	Bus Interface
EC_GPIO67	S5_ENABLE_R	
LOW	HIGH	eSPI
HIGH	HIGH	LPC

← LOGIC

KBC PWR supply at PSL mode

GPIO10 :

Nuvoton KBC PSL Power Switched Logic

1. Enter PSL mode (Entry S5 after 10sec) : 3D3V_AUX_KBC : OFF (KBC PWR supply)
2. At PSL mode (SPEC: S5<10mW)

	EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
PSL Mode (AC or DC)	HIGH	LOW	OFF
PSL Wake (AC or DC):	LOW	HIGH	ON

Main Func = SPI Flash

BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W039
BB1_EVT_MAIN_W043
BB1_EVT_MAIN_W011
BB1_EVT_MAIN_W017
BB1_EVT_MAIN_W020
BB1_SVT_MAIN_W008
BB1_SVT_MAIN_W011
BB1_SVT_MAIN_W012
BB1_SVT_MAIN_L001

18,24 SPI_CS_CPU_N0
18,24,91 SPI_CLK_CPU
15,18,24,91 SPI_SI_CPU
18,24,91 SPI_SO_CPU
15,18 SPI_WP_CPU
15,18 SPI_HOLD_CPU

3D3V_SUS — R2510 1 2 0R0603-PAD-1-GP-U — 3D3V_SPI

3D3V_SPI — R2519 4K7R2J-2-GP — DY

SPI ROM (BIOS1)

BIOS1 (LILY-BIOS-COLAY-GP-U)

SPI_CS_CPU_N0	1 S#	GND 8	
SPI_SO_CPU — R2506 0R2J-2-GP — SPI_SO_ROM	2 DQ1	VCC 7	SPI_HOLD_ROM — R2503 0R2J-2-GP — SPI_HOLD_CPU
SPI_WP_CPU — R2507 0R2J-2-GP — SPI_WP_ROM	3 W#/VPP	HOLD# 6	SPI_CLK_ROM — R2508 0R2J-2-GP — SPI_CLK_CPU
	4 VSS	C 5	SPI_SI_ROM — R2509 0R2J-2-GP — SPI_SI_CPU
		DQ0	

3D3V_SPI

ZZ.00PAD.M41

BIOS1 will use BOM control by co-lay symbol issue
(WINBOND had load code issue)

208MIL SOIC8 (BIOS1) WSON8 / SOP8:		32MB (256Mb) non-vPro	32MB (256Mb) vPro	
~~WINBOND~~	~~W25Q256JWEIQ~~	~~072.25256.0N01~~	~~072.25256.0P01~~	~~(WSON8)~~
MACRONIX	MX25L25673GM2I-08G	072.25673.0001	072.25673.0C01	(SOP8)
GIGADEVICE	GD25B256DYIGR	072.25256.0B03	072.25256.0C03	(WSON8)
MICRON	MT25QL256ABA1EW9-0SIT	072.25256.0E03	072.25256.0D03	(WPDFN8)

SPI ROM Socket (SSKT1)

SSKT1 (SKT-50960-0084L-001-GP)

SPI_CS_CPU_N0	1	8
SPI_SO_ROM	2	7 SPI_HOLD_ROM
SPI_WP_ROM	3	6 SPI_CLK_ROM
	4	5 SPI_SI_ROM

3D3V_SPI — C2502 SCD1U6D3V1KX-GP — 3D3V_SPI

62.10076.051
Co-Layout Design on BIOS1
SPI socket mount in SA stage
SOP 8 package only

Main Func = RTC

18,99 RTC_RST#
18 SRTC_RST#
20 RTC_DET#
19 RTC_TEST
24 RTCRST_ON

3D3V_AUX_S5 — R2514 100R2J-2-GP — 3D3V_AUX_R — D2502 RB530SM-30T2R-GP-U — DY R2515 33K2R2F-GP

RTC CONN

RTCVCC_CONN — R2501 1KR2J-1-GP — RTCVCC_D — D2501 RB530SM-30T2R-GP-U

RTC1 ACES-CON2-20-GP-U 20.F1639.002

Near RTC CONN (RTC1): AFTP2501 AFTP2502 — RTCVCC_CONN

RTC_AUX_S5 — DY C2504 SC1U6D3V1MX-GP

RN2501 SRN20KJ-1-GP

SRTC_RST# — C2501 SC1U10V2KX-1GP — C2503 SC1U10V2KX-1GP

RTC_RST# — G2501 GAP-OPEN — Q2503 LSK3541G1ET2L-GP — RTCRST_ON — R2520 10KR2J-3-GP

ED2501 AZ1043-04F-R7G-GP

(#514849)
Layout: Place at the open door area.

RTCVCC_D — Q2502 LSK3541G1ET2L-GP — Detect Low — RTC_DET# — R2513 100KR2J-1-GP

3D3V_S0 — R2511 10KR2J-L-GP — Test High — RTC_TEST

5V_S0 — R2512 100KR2J-1-GP — RTC_DET#_G

Q2501 LSK3541G1ET2L-GP

LBB-1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	FLASH/RTC
Size A3	Document Number Bumblebee-1 Rev -1
Date: Thursday, May 30, 2019	Sheet 25 of 99

Main Func = Thermal Sensor

Thermal Sensor

BB1_EVT_MAIN_W001
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W050
BB1_EVT_MAIN_W007
BB1_EVT_MAIN_W008
BB1_EVT_MAIN_W017
BB1_EVT_MAIN_W041
BB1_SIT_MAIN_W010
BB1_SIT_MAIN_W022
BB1_SVT_MAIN_W006
BB1_SVT_MAIN_W008

TABLE:

Sensor	Target
U2603	DIMM
U2604	Charger
U2601	SSD
Q2603	CPU DCDC
Q2605	FAN

Close to CPU DCDC

Ch2

Close to FAN

Ch1

Close to DIMM

U2603 NCT7718W-GP 74.07718.0B9

Close to Charger

U2604 NCT7717U-1-GP 74.07717.0BF

Close to SSD Bottom side

U2605 NCT7718W-GP 74.07718.0B9

FAN CONN

FAN1 ACES-CON6-20-GP-U 20.F1639.006

Software Control

Hardware Control

ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)

NCT7717U Table:

R2641	
2.0K	75
7.5K	90
10.5K	100
14.0K	105
18.7K	110

NCT7718W Table:

R2627 \ R2639 R2635 \ R2640	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125

PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

TABLE:

ID	Target	Function
RT2601	PU5101	1D2V_S3
RT2602	PU4801	1V_VCCGT
RT2603	PQ5201	1D05V_SUS
RT2604	PU4701	1V_CPU_CORE
RT2605	PQ4505	5V_S5
RT2606	PQ4506	3D3V_S5
RT2607	PU4404	Charger-Buck
RT2608	PU4406	Charger-Boost

5V *100K/(100K+40K) = 3.57V

U2602 LMV331IDCKRG4-GP 74.00331.A2F

LBB-1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (THERMAL/FAN)

Size: A2 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 26 of 99

BB1_EVT_MAIN_W010
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W017
BB1_SIT_MAIN_W032
BB1_SVT_MAIN_W008

Nearby CODEC

Nearby CODEC

EMC

PLACE UNDER CODEC (ALC3287)

Nearby CODEC

Nearby C2712/C2713/EC2903

For Audio no sound CDE solution

Near U2701

PCB trace width of Mic1-R/Mic1-L(SLEEVE/RING2) are required at least 40 mil for HP crosstalk consideration and its length should be as short as possible

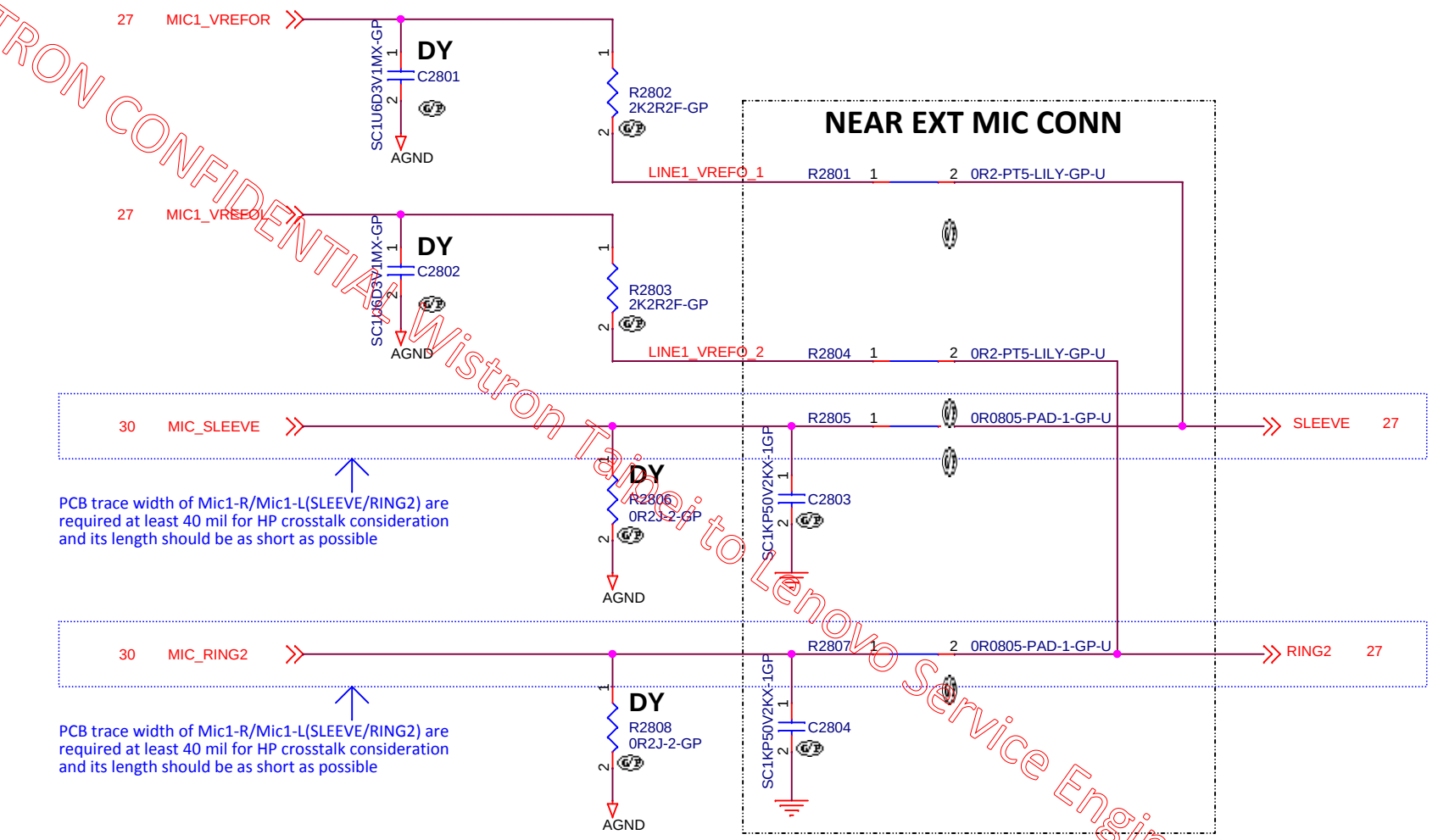
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils

SENSE A: Pin 9 200K : HP Detect
SENSE B: Pin 8 200K : Dock Mic Detect
100K : Dock HP Detect

PCBeep

LBB-1	
Title	AUDIO (CODEC ALC3287)
Size: Custom	Document Number: Bumblebee-1
Rev	-1
Date: Thursday, May 30, 2019	Sheet 27 of 99

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.



LBB-1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (MIC I/F)***

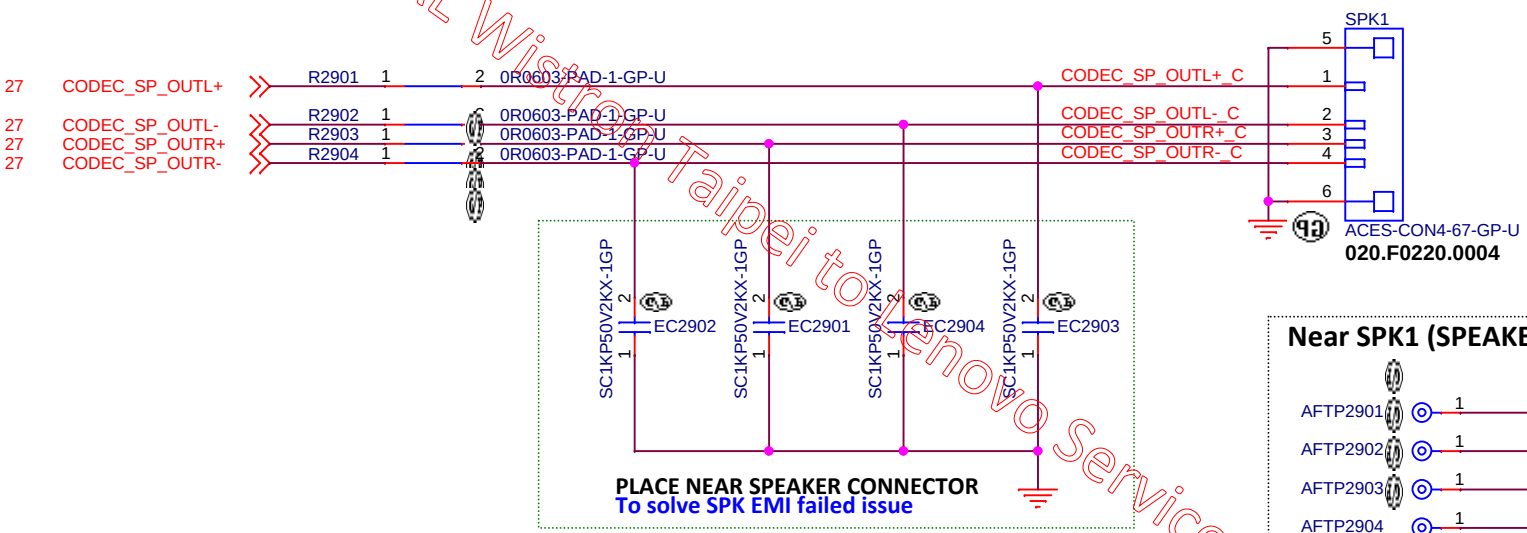
Size	Document Number	Rev
A4	**Bumblebee-1**	**-1**

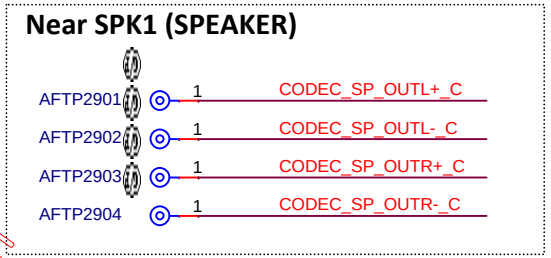
Date: Thursday, May 30, 2019 Sheet 28 of 99

Main Func = AUDIO

BB1_SIT_MAIN_W025
BB1_SVT_MAIN_W008

SPEAKER CONN





LBB-1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO (SPEAKER)		
Size: A4	Document Number: Bumblebee-1	Rev: -1
Date: Thursday, May 30, 2019	Sheet 29 of 99	

BB1_EVT_MAIN_W006
BB1_PVT_MAIN_W034
BB1_SIT_MAIN_W021
BB1_SIT_MAIN_W032
BB1_SVT_MAIN_W008

NEAR AUDIO JACK CONN

27 HP_L_JACK — R3007 1 — 2 0R2-PT5-LILY-GP-U
27 HP_R_JACK — R3008 1 — 2 0R2-PT5-LILY-GP-U
DY C3002 SC100P50V2JN-L-GP
DY C3003 SC100P50V2JN-L-GP
Moat

AUDIO JACK SENSE

CLOSE TO CODEC
6-10 mil trace recommend

HGNDA/HGNDB trace width >70mil, changed to sharp will be better.

3D3V_S0 — R3001 10KR2J-3-GP

Combo Jack

AUD1
3 MIC_RING2
1 HP_L_JACK_CONN
5 3D3V_S0_HPJD
6 HP_JACK_SYS
2 HP_R_JACK_CONN
4 MIC_SLEEVE
MS
Audio(IP/NK_comb)
AUDIO-JK687-GP
AGND

ZZ.00SKT.022
AUD1 will use BOM control to 022.10002.01H1

MIC_RING2 — MIC_RING2 28
HP_L_JACK_CONN
HP_JACK_SYS — R3005 1 — 2 0R2-PT5-LILY-GP-U — HP_JACK_IN 24
HP_R_JACK_CONN
MIC_SLEEVE — MIC_SLEEVE 28

EMC ED3001 AZ5125-02S-R7G-GP 75.05125.07D — Close to AUD1
SC1KP50V2KX-1GP EC3006
DY SC1KP50V2KX-1GP EC3007
EMC ED3002 AZ5125-02S-R7G-GP 75.05125.07D — Close to AUD1
EMC ED3003 AZ5125-02S-R7G-GP 75.05125.07D — Close to AUD1
Moat

R3006 1 — 2 0R0402-PAD-1-GP — AGND
DY EC3005 1 — 2 SCD1U16V2KX-3GP — AGND
Moat

Near AUD1 (AUDIO)

AFTP3001 1 MIC_RING2
AFTP3002 1 HP_L_JACK_CONN
AFTP3003 1 3D3V_S0_HPJD
AFTP3004 1 HP_JACK_SYS
AFTP3005 1 HP_R_JACK_CONN
AFTP3006 1 MIC_SLEEVE
AFTP3007 1 AGND

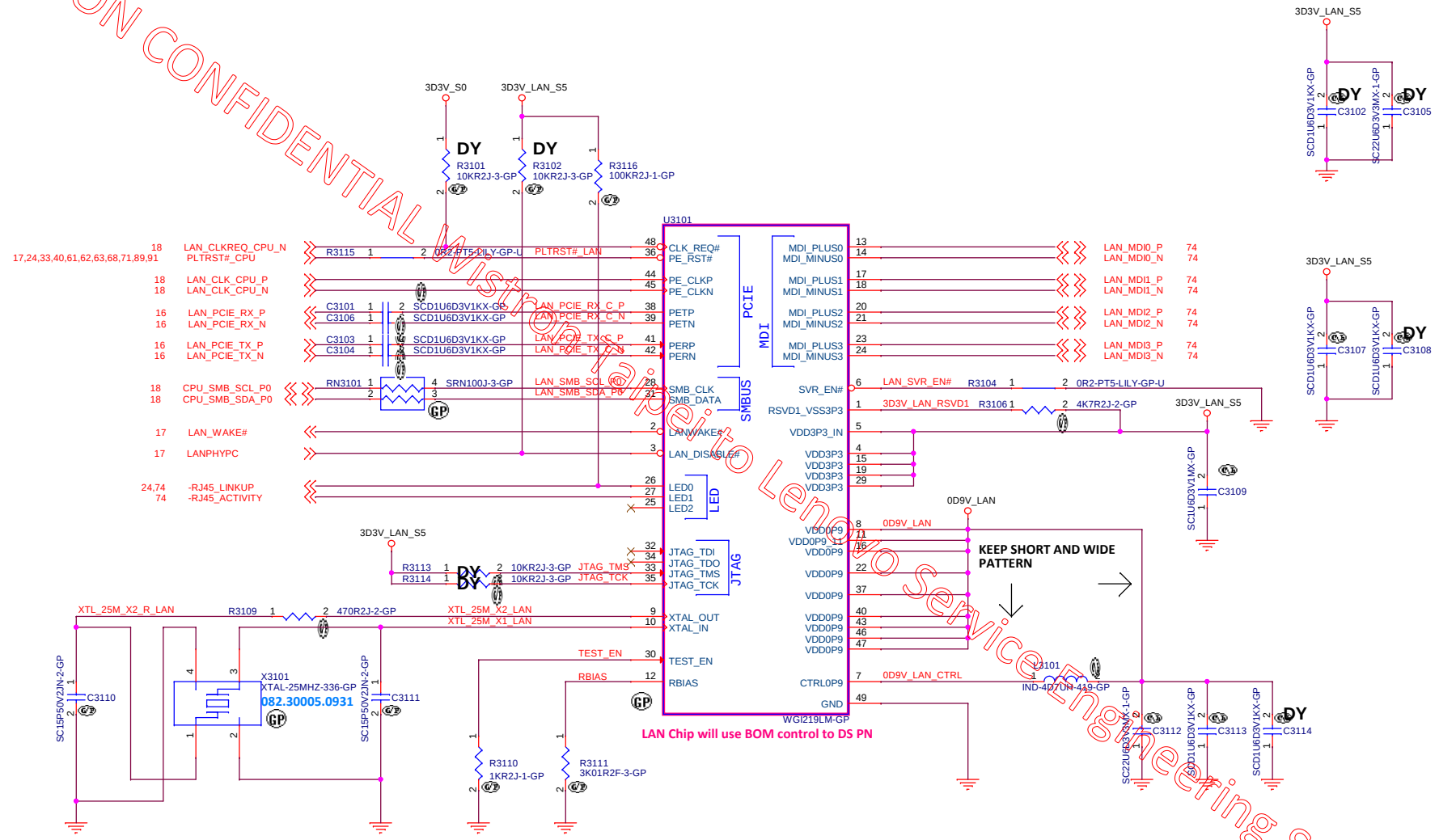
AUDIO JACK SENSE

HP_JACK_SYS — R3002 22KR2J-GP — HP_JACK_SYS_R
Q3001 LSK3541G1ET2L-GP
SENSE_A_SYS_HP 27
R3010 100KR2J-1-GP — AGND
C3001 SC2D2U10V3KX-1GP — AGND
AGND

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO (AUDIO JACK)		
Size: A3	Document Number: Bumblebee-1	Rev: -1
Date: Thursday, May 30, 2019	Sheet 30 of 99	



25MHz (X3101)

TXC	7R25000008	082.30005.0931
HARMONY	X2V025000DC1H-HU	082.30005.0A81

LBB-1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LAN (GIGA_WGI219LM)
Size A3	Document Number Bumblebee-1
Rev	-1
Date: Thursday, May 30, 2019	Sheet 31 of 99

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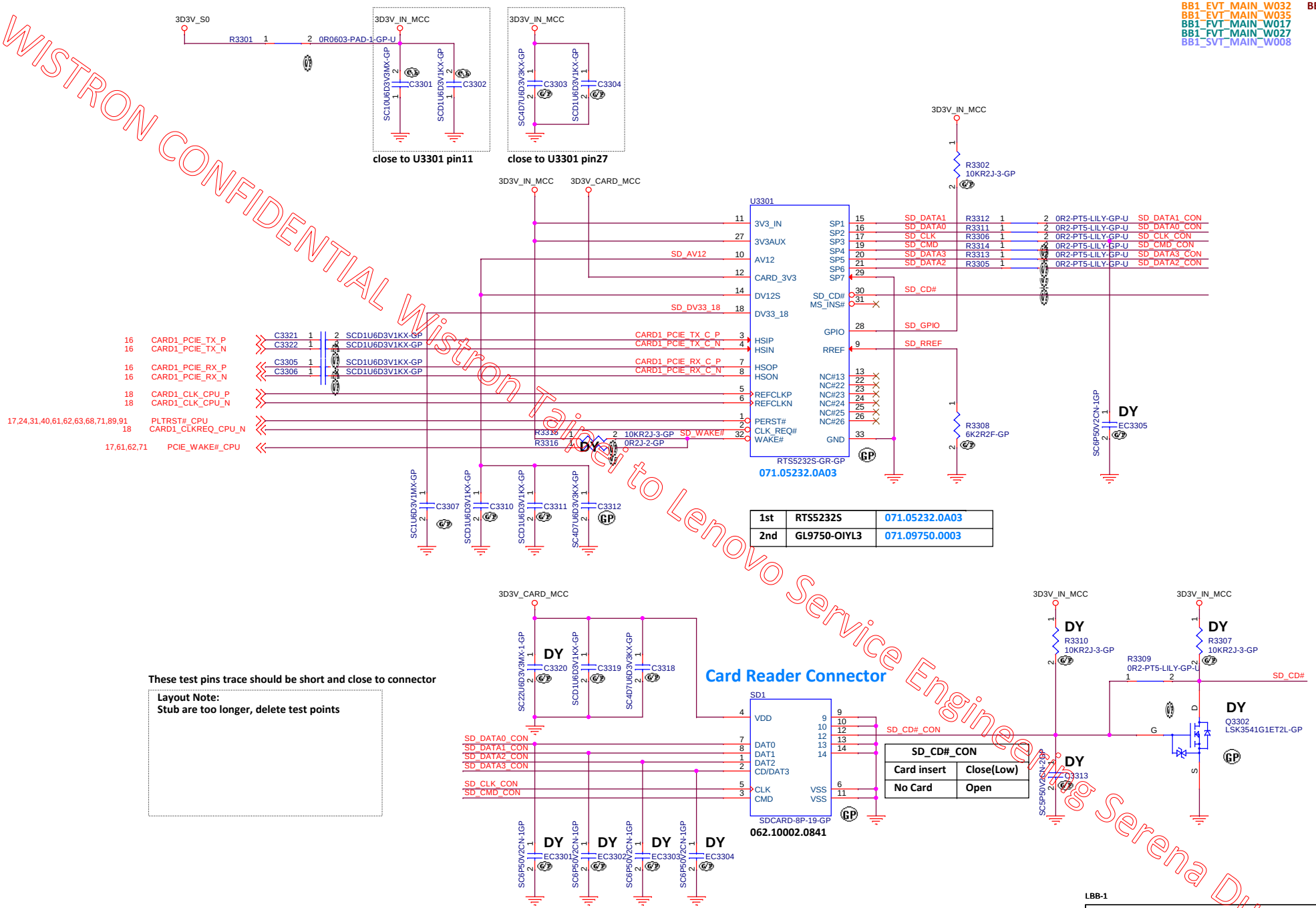
LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RSVD)

Size	Document Number	Rev
A4	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 32 of 99



LBB-1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD READER (SDIO/CONN)

Size	Document Number	Rev
A3	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 33 of 99

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LBB-1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)***

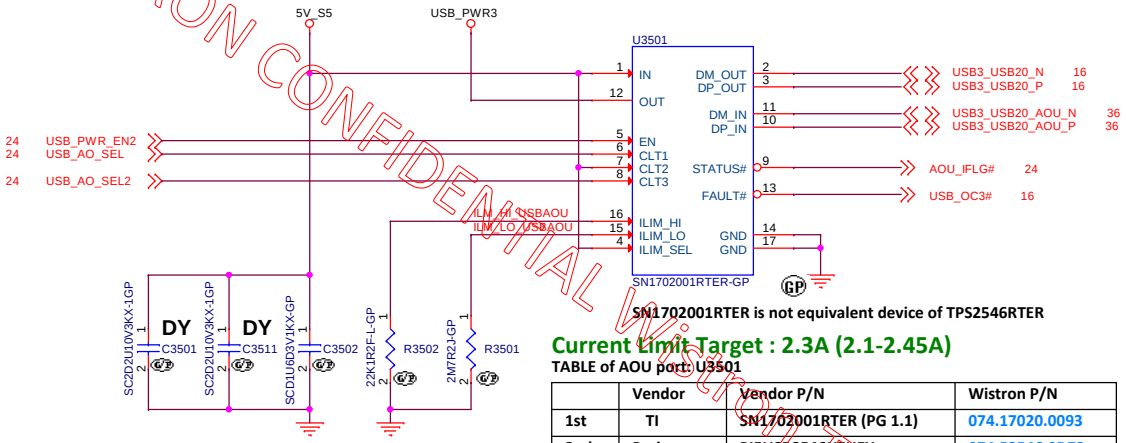
Size	Document Number	Rev
A4	**Bumblebee-1**	**-1**

Date: Thursday, May 30, 2019 Sheet 34 of 99

Main Func = USB Charger

BB1_EVT_MAIN_W032
BB1_FVT_MAIN_W017

For USB3.0 System Port3 (For AOU)



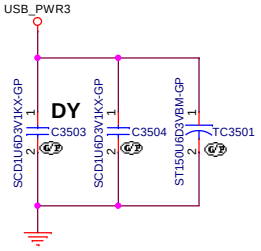
SN1702001RTER is not equivalent device of TPS2546RTER

Current Limit Target : 2.3A (2.1-2.45A)

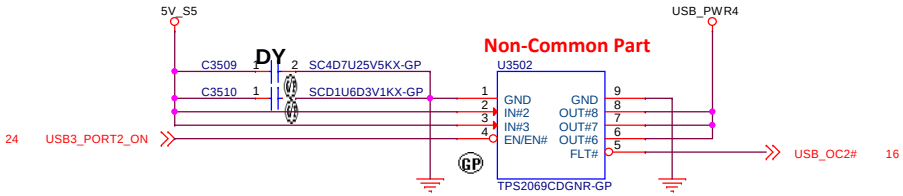
TABLE of AOU port: U3501

	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER (PG 1.1)	074.17020.0093
2nd	Pericom	PI5USB2546HZHEX	074.52546.0D73

Layout Note: Close USB3.0 Port3



For USB3.0 System Port4

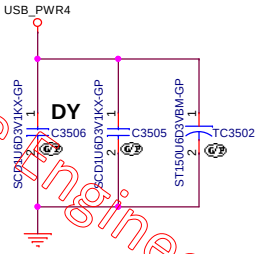


Continous Current Limit 1.5A

TABLE of USB 3.0 port: U3502

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGNR	74.02069.A79
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G
3rd	TI	TPS2001CDGKR	74.02001.A79

Layout Note: Close USB3.0 Port4



LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

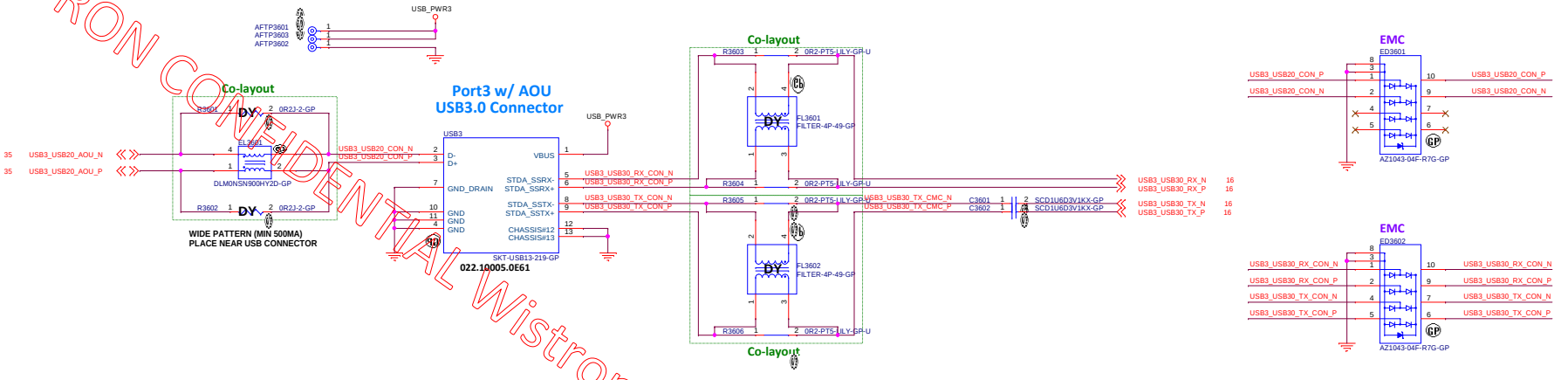
Title: USB (CHARGER/SWITCH)

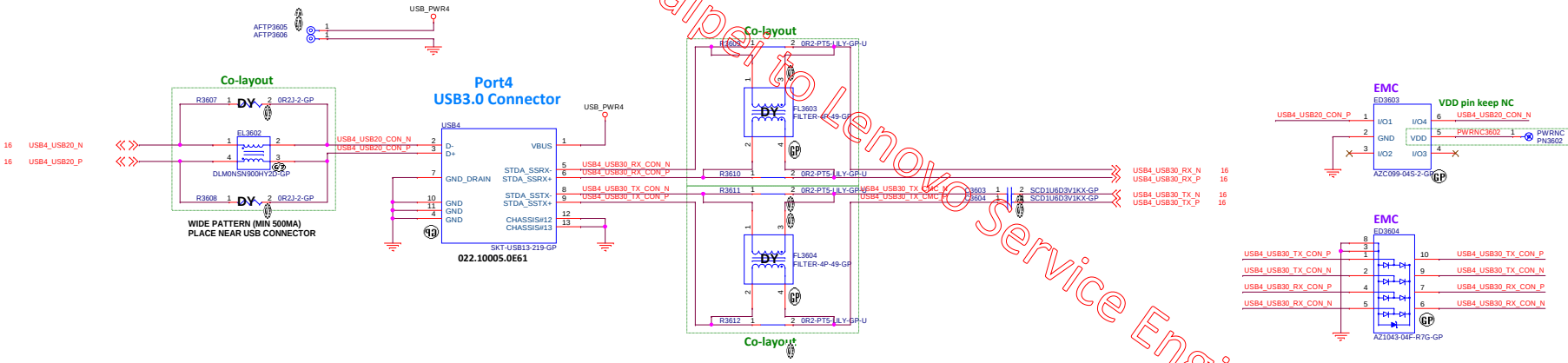
Size: A3 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 35 of 99

Main Func = USB3.0 Port3 w/ AOU
Main Func = USB3.0 Port4

BB1_EVT_MAIN_W024
BB1_EVT_MAIN_W026
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W017
BB1_SVT_MAIN_W008





LBB-1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (USB3.0 CONN)

Size	Document Number	Rev
A2	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 36 of 99

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LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (RSVD)

Size	Document Number	Rev
A4	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 37 of 99

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LBB-1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-1**	**-1**

Date: Thursday, May 30, 2019 Sheet 38 of 99

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LBB-1

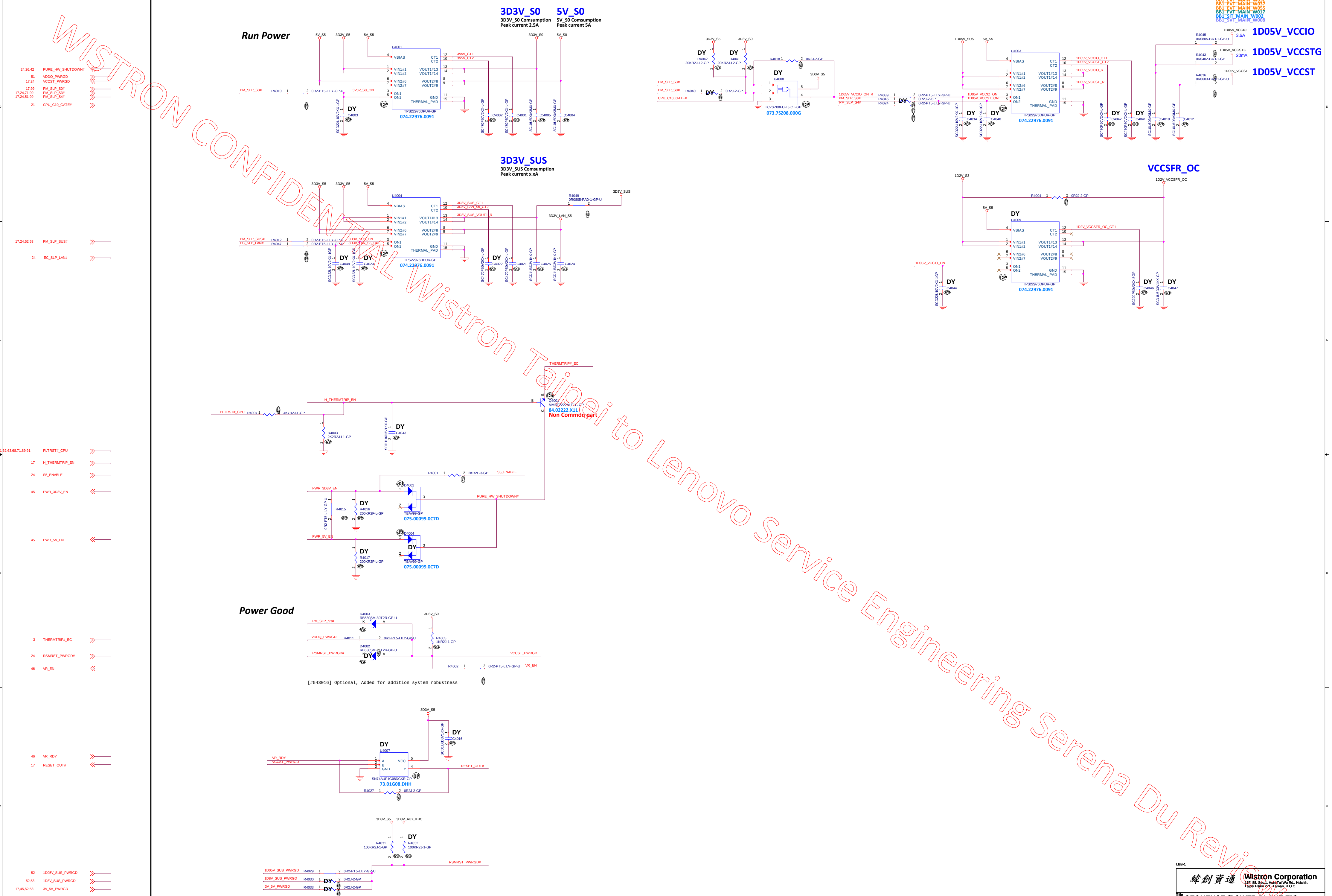
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SEQUENCE (RSVD)

Size	Document Number	Rev
A4	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 39 of 99

Power Plane & Sequence



LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SEQUENCE (POWER PLANE EN)

Size: A1 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 40 of 99

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LBB-1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SEQUENCE (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-1**	**-1**

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BB1_EVT_MAIN_W022
BB1_EVT_MAIN_W031
BB1_EVT_MAIN_W007
BB1_EVT_MAIN_W017
BB1_SIT_MAIN_W038
BB1_SVT_MAIN_W008
BB1_SVT_MAIN_W013

Q4201, Q4202, Q4205, Q4206

1st	VISHAY	SI7153DN-T1-GE3	084.07153.0037
2nd	AOS	AONR21357	084.21357.0A37
~~3rd~~	~~AOS~~	~~AON7405~~	~~084.07405.0A01~~
~~4th~~	~~PANJIT~~	~~PJQ4407P~~	~~084.04407.0A01~~

EOL soon
had supply issue (OBS part)

USBC_VBUS20 → F4201 FUSE-5A32V-15-GP → USBC_VBUS20_F → Q4201 / Q4202 (SI7153DN-T1-GE3-GP) → USB1_VBUS_A → VINT20_IN

Non-Common Part

C4201 SCD1U25V2KX-GP

USB1_HV_GATE2_G: R4201 100R2J-2-GP; R4202 100KR2F-L1-GP; C4209 SCD1U25V2KX-GP (DY)

USB1_HV_GATE1_G: R4203 100R2J-2-GP; C4202 SCD047U25V2KX-GP; C4210 SC1KP50V2KX-1GP

USB1_HV_GATE_D_R → R4204 10KR2F-2-GP → USB1_HV_GATE_D

ET4201 SE3V26VM-11-GP — LAN ISN Test Related

C4211 SCD0U16DV2KX-1GP

3D3V_LDO_PD → R4215 10KR2J-3-GP → 3D3V_LDO_PD_ADT → D4201 RB530SM-30T2R-GP-U → R4213 100KR1J-GP (DY) → 3D3V_LDO_PD

73 USBC_HV_GATE → R4209 0R2J-2-GP → USB1_HV_GATE_R → Q4203 LSK3541G1ET2L-GP

R4210 100KR2J-1-GP; C4212 SCD1U16D3V1KX-GP (DY)

USB1_-PWRSHUTDOWN_D

24,26,40 PURE_HW_SHUTDOWN# → R4211 0R2-PT5-LILY-GP-U → PURE_HW_SHUTDOWN#_A_R → Q4204 LSK3541G1ET2L-GP

DOCK_VBUS20 → F4202 FUSE-5A32V-15-GP → DOCK_VBUS20_F → Q4205 / Q4206 (SI7153DN-T1-GE3-GP) → DK1_VBUS_A → VINT20_IN

Non-Common Part

C4205 SCD1U25V2KX-GP

DK1_HV_GATE2_G: R4205 100R2J-2-GP; R4206 100KR2F-L1-GP; C4214 SCD1U25V2KX-GP (DY)

DK1_HV_GATE1_G: R4207 100R2J-2-GP; C4206 SCD047U25V2KX-GP; C4215 SC1KP50V2KX-1GP

DK1_HV_GATE_D_R → R4208 10KR2F-2-GP → DK1_PWRSHUTDOWN#_D

C4207 SCD1U25V5MX-7-GP — LOW_NOISE — Discrete Type Noise Related — LAN ISN Test Related

C4213 SCD01U16DV2KX-1GP

73 DOCK_HV_GATE → R4212 0R2J-2-GP → DK1_HV_GATE_R → Q4207 LSK3541G1ET2L-GP

R4214 100KR2J-1-GP; C4216 SCD1U16D3V1KX-GP (DY)

USB1_-PWRSHUTDOWN_D

LBB-1

緯創資通 Wistron Corporation
21F., 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

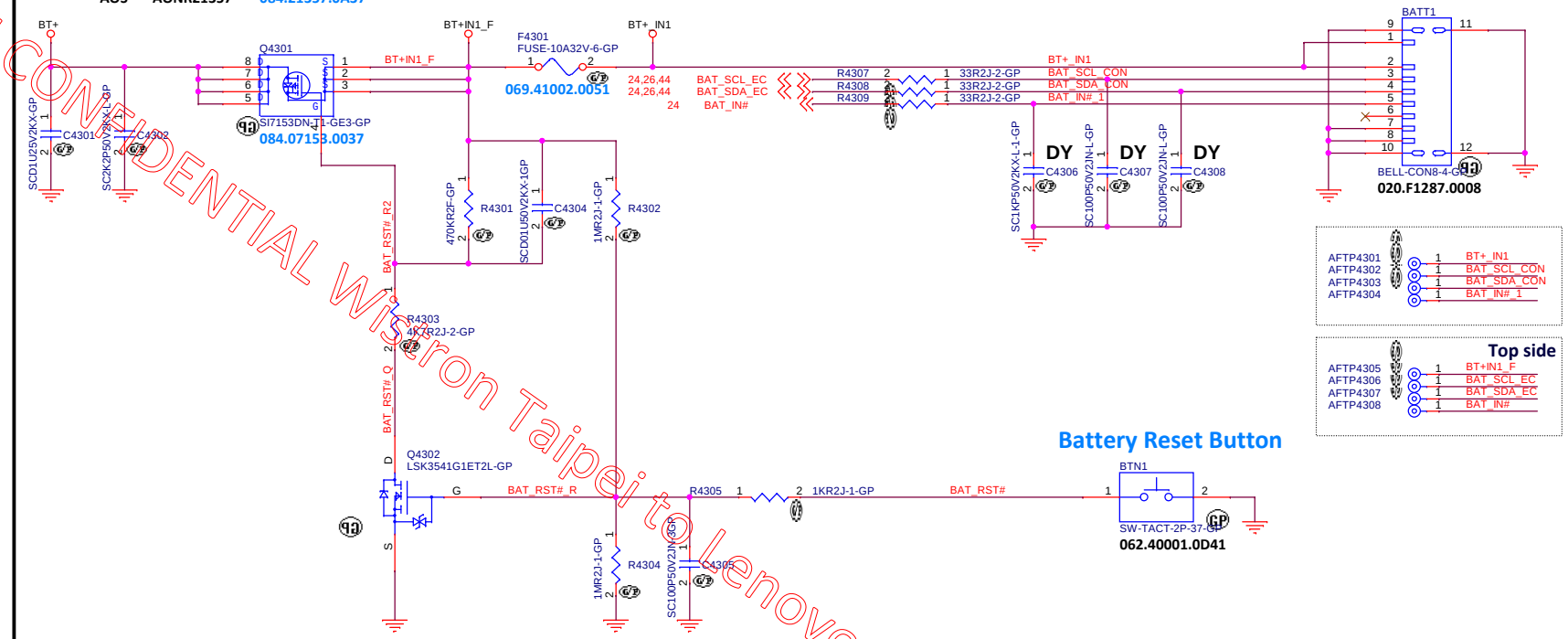
Title	INT IO (DC-IN)	
Size: A2	Document Number: Bumblebee-1	Rev: -1
Date: Thursday, May 30, 2019	Sheet 42 of 99	

OFFPAGE

BB1_EVT_MAIN_W006
BB1_EVT_MAIN_W009
BB1_EVT_MAIN_W012
BB1_EVT_MAIN_W015
BB1_EVT_MAIN_W031
BB1_EVT_MAIN_W034

Q4301:
VISHAY SI7153DN 084.07153.0037
AOS AONR21357 084.21357.0A37

Main Battery Connector



Battery Reset Button

LBB-1

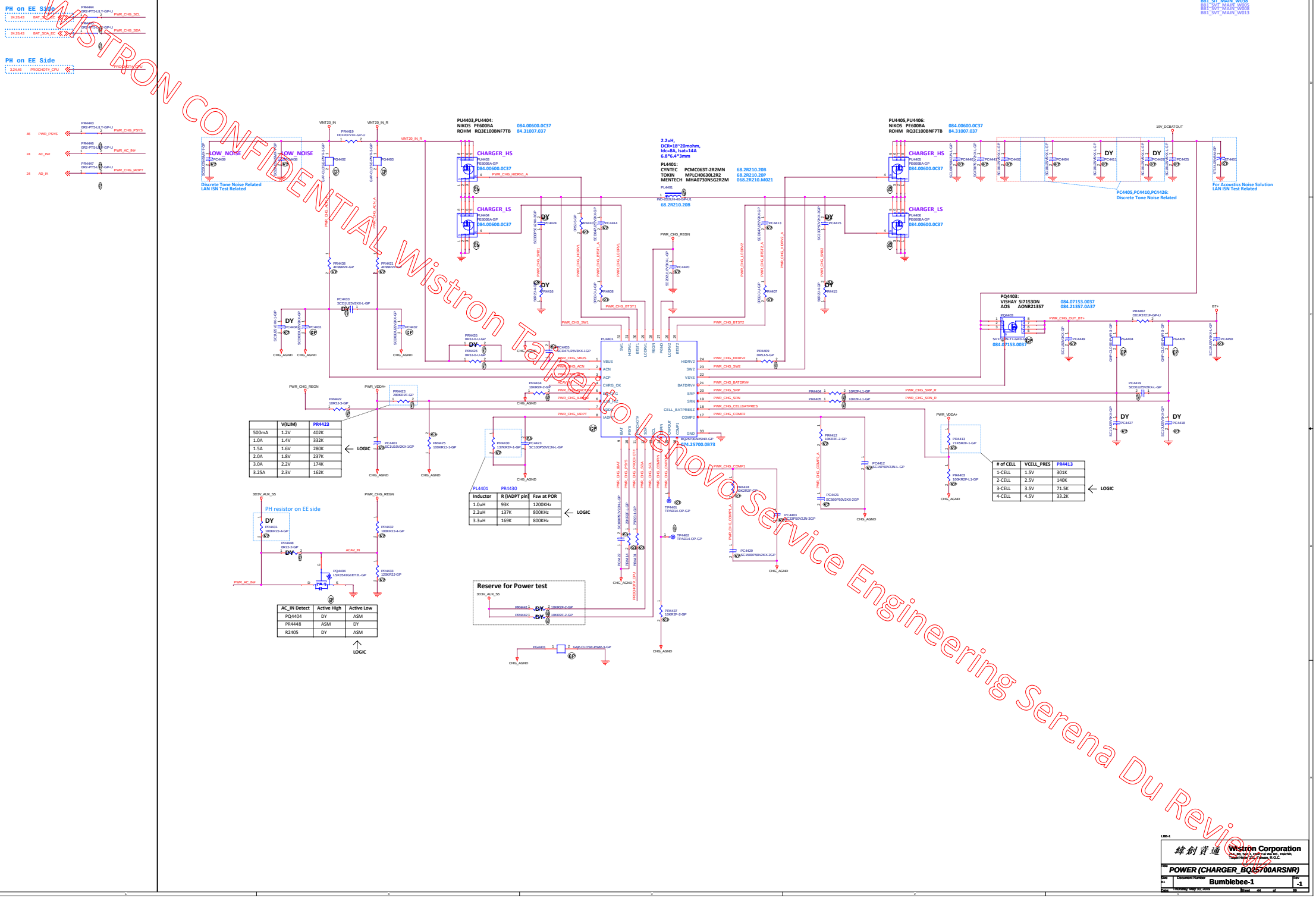
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (BATT CONN)

Size: A3 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 43 of 99

OFFPAGE - PIC - EE



V(ILIM)	PR4423
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

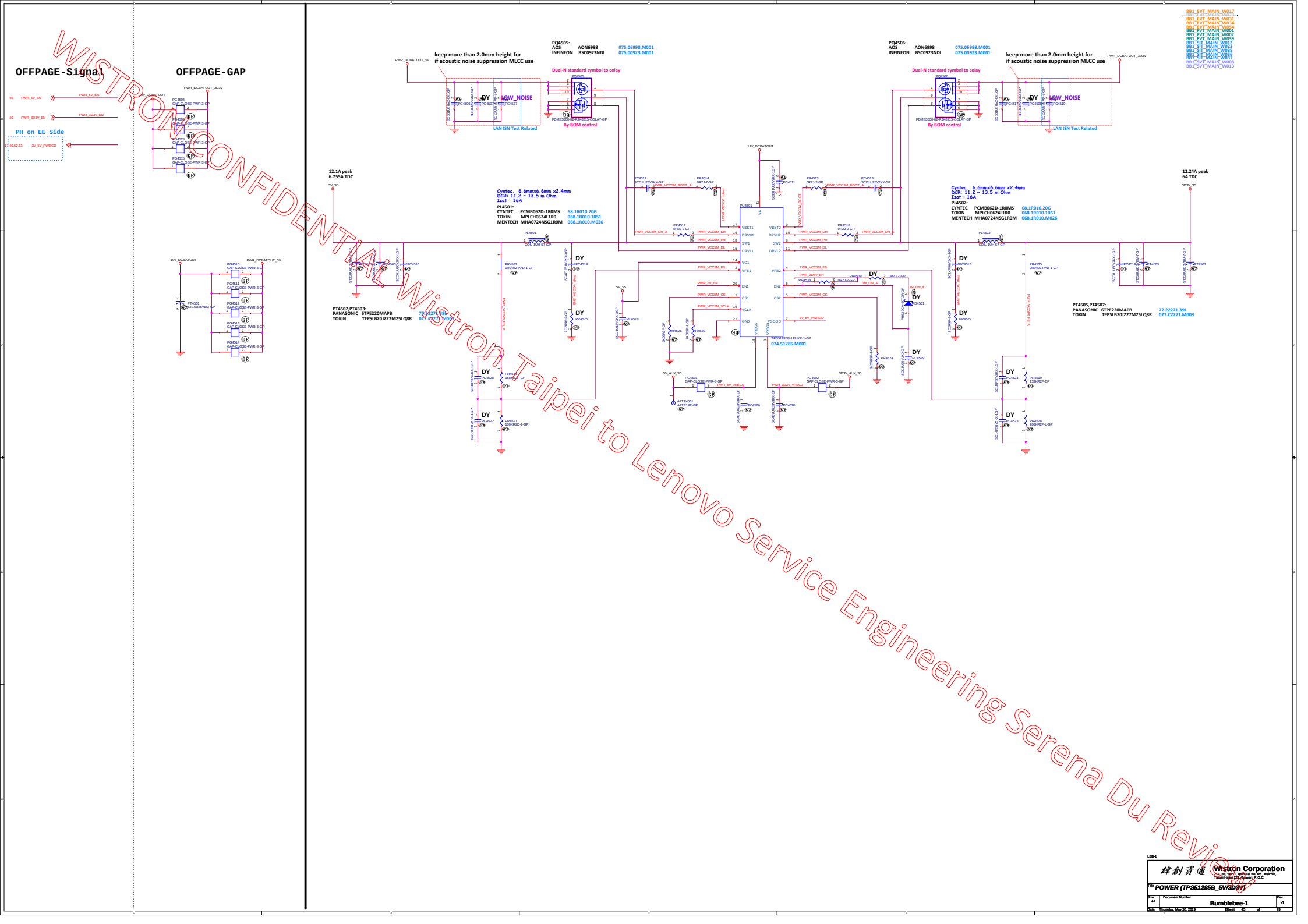
PL4401 PR4430

Inductor	R (IADPT pin)	Fsw at POR
1.0uH	93K	1200KHz
2.2uH	137K	800KHz
3.3uH	169K	800KHz

# of CELL	VCELL_PRES	PR4413
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

AC_IN Detect	Active High	Active Low
PQ4404	DY	ASM
PR4448	ASM	DY
R2405	DY	ASM

BB-1
緯創資通 Wistron Corporation
3F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: POWER (CHARGER_BQ25700ARSNR)
Size: A1
Document Number: Bumblebee-1
Rev: -1
Date: Thursday, May 30, 2013
Sheet 64 of 89



Wistron Corporation			
Title: POWER (TPS51285B_5V/3D3V)			
Size: A1	Document Number: Bumblebee-1	Rev: -1	
Date: Thursday, May 30, 2019	Sheet 45 of 89		

OFFPAGE

40 VR_EN
7 SVID_ALERT#_CPU
7 SVID_CLK_CPU
7 SVID_DATA_CPU
44 PWR_PSYS
8 VCCGT_SENSE
8 VSSGT_SENSE
7 VCCCORE_SENSE
7 VSSCORE_SENSE
8 VCCSA_SENSE
8 VSSSA_SENSE
40 VR_RDY
3,24,44 PROCHOT#_CPU
47,48,50 DRVON
48 1V_VCCGT_PWM_1A
48 1V_VCCGT_SW_1A
48 1V_VCCGT_CSN_1A
47 1V_CPU_CORE_PWM1_2PH
47 1V_CPU_CORE_PWM2_2PH
47 1V_CPU_CORE_CSP1
47 1V_CPU_CORE_CSP2
47 1V_CPU_CORE_CSN1
47 1V_CPU_CORE_CSN2
50 PWR_VCCSA_PWM
50 PWR_VCCSA_CSP
50 PWR_VCCSA_CSN

EE side Link
SVID Pull High V

1D05V_VCCST
PG4602 GAP-CLOSE-PWR-3-GP
PWR_CORE_VCCST

WHL U42 15W

	IA	GT	SA
Imax	70A	31A	6A
LL	1.8m	3.1m	10.3m

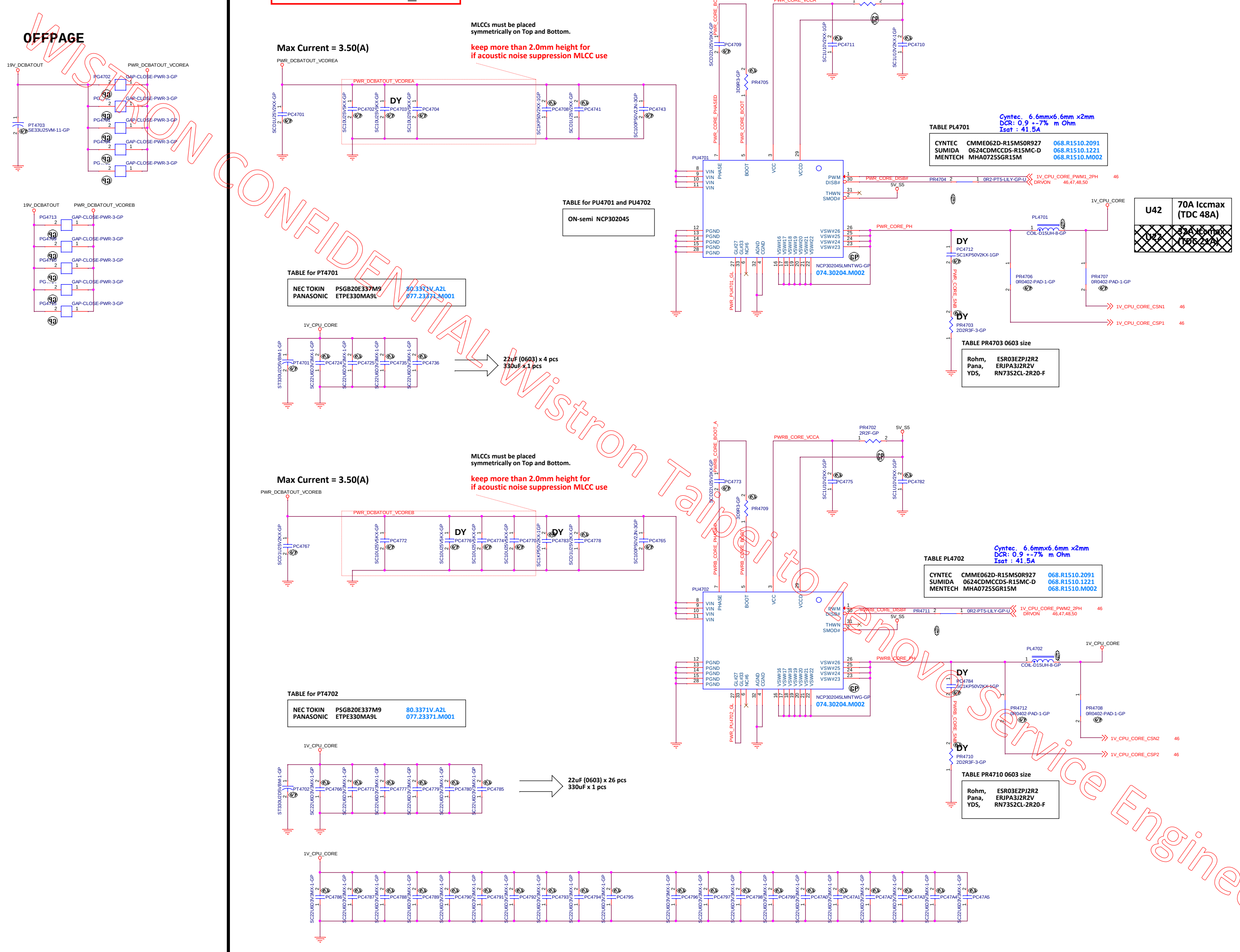
PLACE NEAR TO PU4501

PLACE CLOSE TO VCCPUCORE PL4702
PLACE CLOSE TO VCCPUCORE PU4701
PLACE CLOSE TO VCCGT PL4802
PLACE CLOSE TO VCCGT PU4801
PLACE CLOSE TO VCCSA PL4902

NCP81218MNTXG-1-GGY
074.81218.M001

Main Func = CPU_CORE

BB1_EVT_MAIN_W017
BB1_EVT_MAIN_W031
BB1_FVT_MAIN_W001
BB1_SIT_MAIN_W006
BB1_SIT_MAIN_W012
BB1_SIT_MAIN_W023
BB1_SIT_MAIN_W035
BB1_SVT_MAIN_W008



LBB-1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (NCP302045_CPUCORE)	
Size A1	Document Number: Bumblebee-1	Rev -1
Date: Thursday, May 30, 2019	Sheet 47 of 99	

BB1_EVT_MAIN_W017
BB1_SIT_MAIN_W006
BB1_SIT_MAIN_W012
BB1_SIT_MAIN_W035
BB1_SVT_MAIN_W008

OFFPAGE

19V_DCBATOUT
PWR_DCBATOUT_VCCGTA
PT4802 SE33U25VM-11-GP

Main Func = CPU_CORE

MLCCs must be placed symmetrically on Top and Bottom.

Max Current = 3.88(A)

keep more than 2.0mm height for if acoustic noise suppression MLCC use

PWR_DCBATOUT_VCCGTA
PC4801 SCD10U25V6KX-GP
PC4802 PC4803 PC4804 PC4805 PC4806 SC10U25V6KX-GP
DY
PC4855 SCD1U25V6KX-GP
PC4859 SC10P50V2JN-3GP
SCK1KP50V2KX-1GP

PU4801 NCP302045LMNTWG-GP
074.30204.M002
VIN PHASE BOOT VCC VCCD PWM DISB# THWN SMOD# PGND GL/GT GL/G3 N/C/I6 AGND C/GND VSW#16 VSW#17 VSW#18 VSW#19 VSW#20 VSW#21 VSW#22 VSW#23 VSW#24 VSW#25 VSW#26

PWR_VCCGT_PHASED
PWR_VCCGT_BOOTA
PWR_VCCGT_BOOTA_G
PWR_VCCGT_VCC
PR4801 2R2F-GP
PR4802 3D9R3-GP
PC4820 SCD22U25V2KX-GP
PC4821 SC1U10V2KX-1GP
PC4819 SC1U10V2KX-1GP
5V_S5

TABLE PL4801

CYNTEC	CMME062D-R15MS0R927	068.R1510.2091
SUMIDA	0624CDMCCDS-R15MC-D	068.R1510.1221
MENTECH	MHA0725SGR15M	068.R1510.M002

Cyntec 6.6mmx6.6mm x2mm
DCR: 0.9 +-7% m Ohm
Isat : 41.5A

TABLE for PU4801

ON-semi NCP302045

*PWR_VCCGT_DISB#
PR4804 0R2-PT5-LILY-GP-U
1V_VCCGT_PWM_1A 46
DRVON 46,47,50

31A Iccmax
(TDC: 18A)

PWR_VCCGT_PH
PL4802 COIL-D15UH-8-GP
1V_VCCGT
PR4805 0R0402-PAD-1-GP
PR4806 0R0402-PAD-1-GP
1V_VCCGT_CSN_1A 46
1V_VCCGT_SW_1A 46

DY
PC4832 SC1KP50V2KX-1GP
PWR_VCCGT_SW
DY
PR4803 2D2R3F-3-GP

TABLE PR4803 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

TABLE for PT4801

NEC TOKIN	PSGB20E337M9	80.3371V.A2L
PANASONIC	ETPE330MA9L	077.23371.M001

1V_VCCGT
PT4801 ST330UD25V6M-1-GP
PC4809 PC4810 PC4811 PC4812 PC4813 PC4814 PC4815 PC4816 PC4817 PC4818 PC4823 PC4824 PC4825 PC4826 PC4828 PC4829 PC4831 SC22U6D3V3MX-1-GP

1V_VCCGT
PC4834 PC4835 PC4841 PC4836 PC4837 PC4839 PC4833 SC22U6D3V3MX-1-GP

For U42 22uF (0603) x 27 pcs
330uF x 1pcs
For U22 22uF (0603) x 25 pcs
330uF x 1 pcs

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (NCP302045_VCCGT)

Size	Document Number	Rev
A2	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 48 of 99

Main Func = CPU_CORE

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LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RSVD)

Size	Document Number	Rev
A4	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 49 of 99

Main Func = CPU_CORE

OFFPAGE

19V_DCBATOUT
PWR_DCBATOUT_VCCSA
PG5002 GAP-CLOSE-PWR-3-GP
PG5003 GAP-CLOSE-PWR-3-GP

PR5013 2D2R3-1-U-GP
PWR_VCCSA_BST_RC
PWR_VCCSA_BST
PC5008 SCD22U25V3KX-GP
PU5001
BST PWM EN VCC DRVH SW GND DRVL GND
NCP81253MNTBG-1-GP
074.81253.0AE3
46 PWR_VCCSA_PWM
46,47,48 DRVON
5V_S5
PC5001 SC2D2U10V3KX-L-GP
PWR_VCCSA_DRVH
PWR_VCCSA_SW
PWR_VCCSA_DRVL

PU5002,PU5003:
NIKOS PE606BA 084.00606.0037
VISHAY SIS412DN 84.00412.037

VCCSA_HS
PU5002 PE606BA-GP
084.00606.0037
VCCSA_LS
PU5003 PE606BA-GP
084.00606.0037

PWR_DCBATOUT_VCCSA
PC5029 SC10U25V5KX-L-GP
PC5027 SC10U25V5KX-L-GP
PC5002 SCD1U25V2KX-L-GP

PR5014 2D2R5F-2-GP
PWR_VCCSA_SNUB
PC5031 SC1KP50V2KX-1GP
PG5021 GAP-CLOSE-PWR-3-GP

PL5001
IND-D47UH-46-GP
1V_VCCSA
PG5022 GAP-CLOSE-PWR-3-GP

46 PWR_VCCSA_CSP
46 PWR_VCCSA_CSN

Cyntec 6.6mmx6.6mm x2mm
DCR: 7.3 - 8.4 m Ohm
Isat : 18A
PL5001:
CYNTEC PCMB061H-R47MS 68.R4710.20C
TOKO FDV0620-H-R47M 68.R471A.10D
MENTECH MHA0718NSGR47M 068.R4710.M012

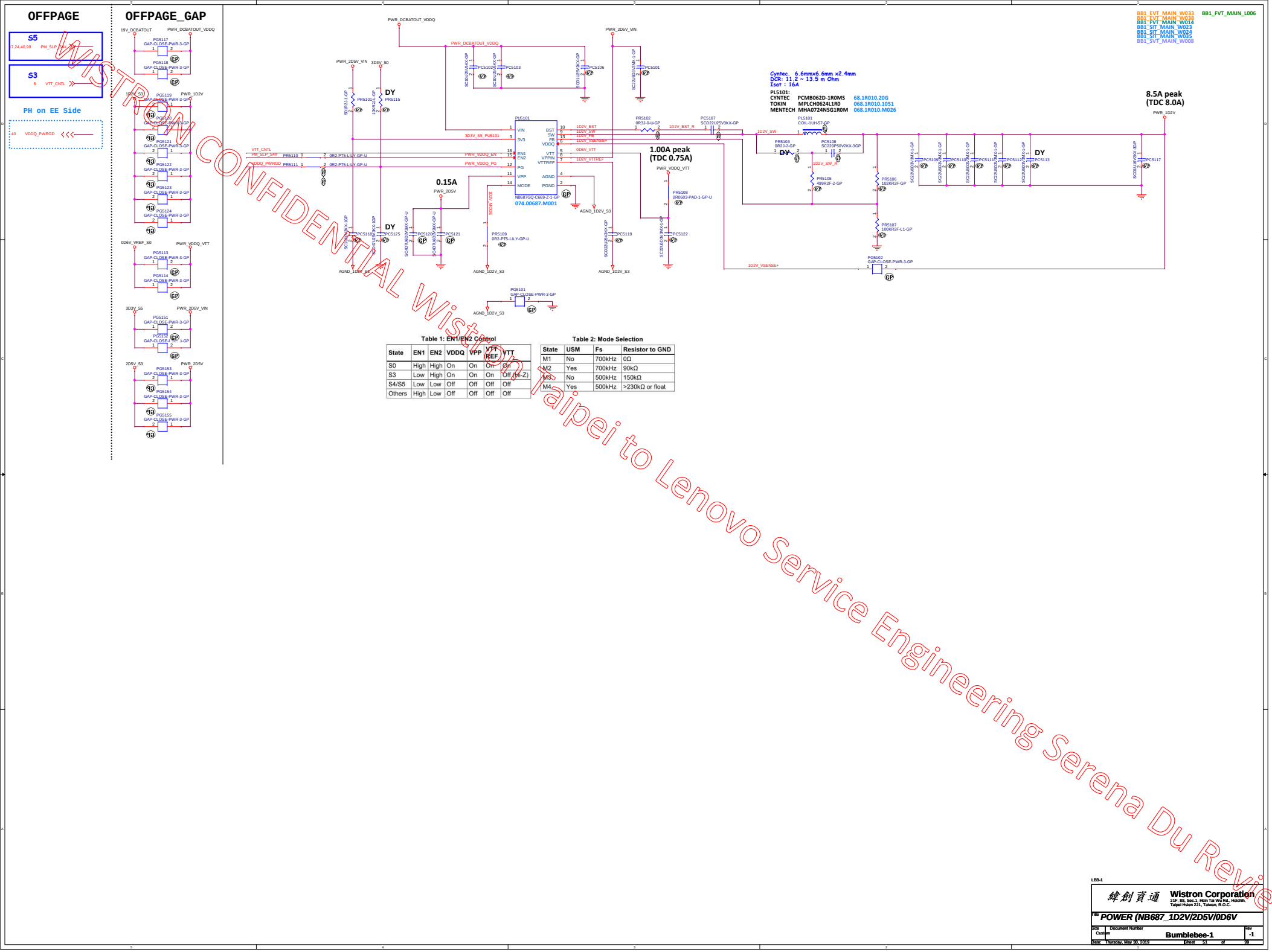
TDC: 4A
Iccmax: 6A
OCP > 6.75A

BB1_FVT_MAIN_W001
BB1_FVT_MAIN_W003
BB1_SIT_MAIN_W008
BB1_SIT_MAIN_W023
BB1_SIT_MAIN_W035

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (NCP81253MN_VCCSA)
Size: A3 | Document Number: Bumblebee-1 | Rev: -1
Date: Thursday, May 30, 2019 | Sheet 50 of 99



State	EN1	EN2	VDDQ	VPP	VTT REF	VTT
S0	High	High	On	On	On	On
S3	Low	High	On	On	On	Off (Hi-Z)
S4/S5	Low	Low	Off	Off	Off	Off
Others	High	Low	Off	Off	Off	Off

State	USM	Fs	Resistor to GND
M1	No	700kHz	0Ω
M2	Yes	700kHz	90kΩ
M3	No	500kHz	150kΩ
M4	Yes	500kHz	>230kΩ or float

OFFPAGE

PH on EE Side

40 1D05V_SUS_PWRGD — PR5210 0R2-PT5-LILY-GP-U — PWR_1D05V_PG

40,53 1D8V_SUS_PWRGD — PR5211 0R2-PT5-LILY-GP-U — PWR_1D05V_EN

17,24,40,53 PM_SLP_SUS# — PR5212 0R2J-2-GP DY

17,40,45,53 3V_5V_PWRGD — PR5213 0R2J-2-GP DY

OFFPAGE_GAP

19V_DCBATOUT — PWR_DCBATOUT_1D05V

PG5202 GAP-CLOSE-PWR-3-GP
PG5203 GAP-CLOSE-PWR-3-GP
PG5204 GAP-CLOSE-PWR-3-GP
PG5205 GAP-CLOSE-PWR-3-GP

1D05V_SUS — PWR_1D05V

PG5206 GAP-CLOSE-PWR-3-GP
PG5207 GAP-CLOSE-PWR-3-GP
PG5208 GAP-CLOSE-PWR-3-GP
PG5209 GAP-CLOSE-PWR-3-GP
PG5210 GAP-CLOSE-PWR-3-GP
PG5211 GAP-CLOSE-PWR-3-GP
PG5214 GAP-CLOSE-PWR-3-GP
PG5215 GAP-CLOSE-PWR-3-GP
PG5212 GAP-CLOSE-PWR-3-GP
PG5213 GAP-CLOSE-PWR-3-GP

BB1_EVT_MAIN_W031
BB1_EVT_MAIN_W033
BB1_EVT_MAIN_W056
BB1_EVT_MAIN_W038
BB1_SIT_MAIN_W035
BB1_SVT_MAIN_W008

PQ5201
AOS AON6998 075.06998.M001
INFINEON BSC0923NDI 075.00923.M001
Dual-N standard symbol to colay

PQ5201 — FDMS3600-02-RJK0215-COLAY-GP
By BOM control

PWR_DCBATOUT_1D05V
PC5202 SC10U25V5KX-L-GP
PC5203 SC10U25V5KX-L-GP
PC5204 SCD1U25V2KX-L-GP

Cyntec. 6.6mmx6.6mm x2.4mm
DCR: 11.2 ~ 13.5 m Ohm
Isat : 16A
PL5201:
CYNTEC PCMB062D-1R0MS 68.1R010.20G
TOKIN MPLCH0624L1R0 068.1R010.1051
MENTECH MHA0724NSG1R0M 068.1R010.M026

Icc(max):
Peak : 13.518A
TDC : 9.452A

OCP = 18A

3D3V_S5 — PR5202 10KR2J-3-GP DY

PU5201 RT8237CZQW-2-1-GP
074.08237.0B73
PGOOD, CS, EN, FB, RF, GND, BOOT, UGATE, PHASE, VCC, LGATE
PWR_1D05V_PG, PWR_1D05V_CS, PWR_1D05V_EN, PWR_1D05V_FB, PWR_1D05V_RF
PWR_1D05V_BOOT, PWR_1D05V_HG, PWR_1D05V_PH, PWR_1D05V_LG

PR5201 2D2R3-1-U-GP
PC5205 SCD1U25V2KX-GP
PWR_1D05V_BOOT_A
5V_S5
PC5206 SC1U10V2KX-L1-GP

PR5207 470KR2F-GP
PR5208 43K2R2F-L-GP
PC5207 SC1KP50V2KX-1-GP DY

PWM Frequency setting
RF=470K
PWM Frequency=290K Hz

PL5201 COIL-1UH-57-GP
PWR_1D05V
PG5201 GAP-CLOSE-PWR-3-GP
PC5201 SCD1U25V2KX-L-GP
PT5201 ST220U2VDM-5-GP

PWR_1D05V_FB_A
PR5208 10KR2F-2-GP
PC5209 SC18P50V2JN-1-GP DY
PWR_1D05V_FB
PR5209 20KR2F-L-GP

Vout = 0.704 * (1+ 10/20) = 1.056

Table 1. RF Connection and Switching Frequency

R_{RF} (kΩ)	Switching Frequency (kHz)
470kΩ	290
200kΩ	340
100kΩ	380
39kΩ	430

<--- LOGIC

Note : For DEM, connect R_{RF} to GND; for CCM, connect R_{RF} to PGOOD.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is 0.704V (typ.).

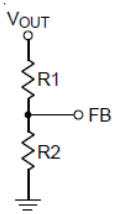
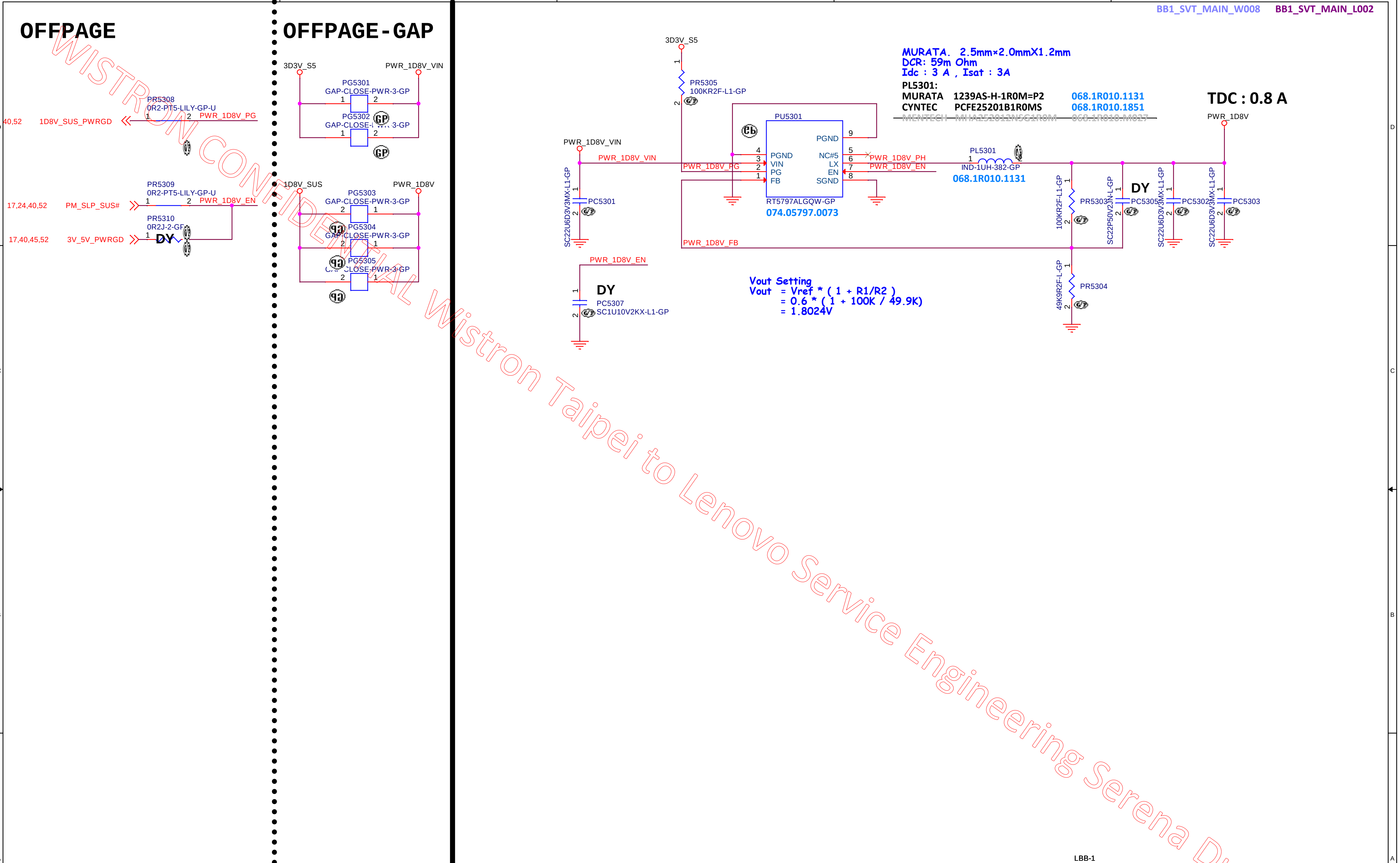


Figure 4. Setting V_{OUT} with a Resistive Voltage Divider

LOB-1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT8237C_1D05V)
Size: Custom | Document Number: Bumblebee-1 | Rev: -1
Date: Thursday, May 30, 2019 | Sheet 52 of 99



LBB-1

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER (RT5797_1D8V)**

Size	Document Number	Rev
A3	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 53 of 99

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LBB-1

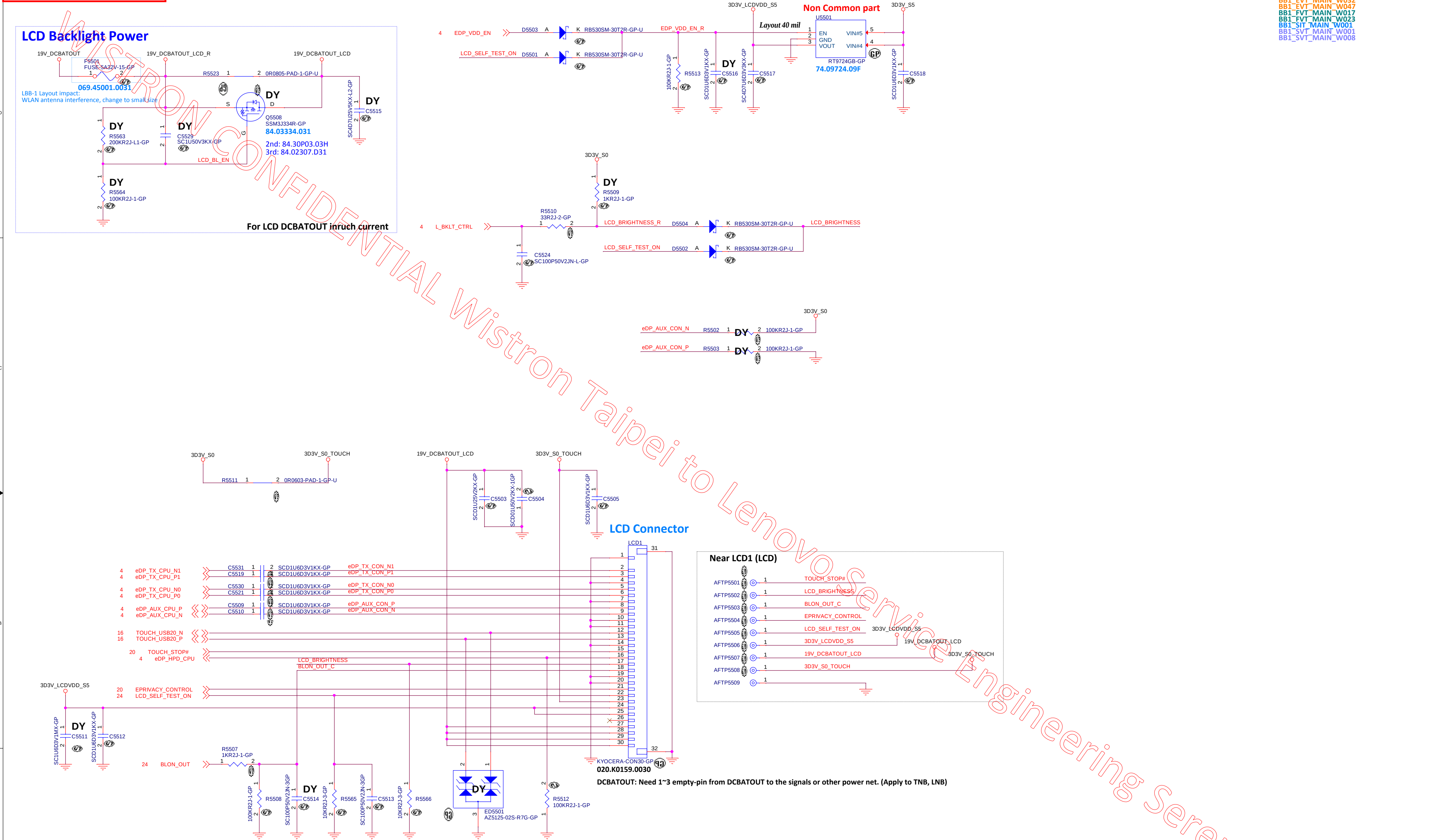
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RSVD)

Size	Document Number	Rev
A4	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 54 of 99

Main Func = LCD



LCD Backlight Power
19V_DCBATOUT
19V_DCBATOUT_LCD_R
19V_DCBATOUT_LCD
F5501
FUSE-5A32V-15-GP
069.45001.0031
LBB-1 Layout impact:
WLAN antenna interference, change to small size
R5523
0R0805-PAD-1-GP-U
Q5508
SSM3J334R-GP
84.03334.031
2nd: 84.30P03.03H
3rd: 84.02307.D31
R5563
200KR2J-L1-GP
C5529
SC1U50V3KX-GP
C5515
SC4D7U25V5KX-L2-GP
LCD_BL_EN
R5564
100KR2J-1-GP
For LCD DCBATOUT inruch current
EDP_VDD_EN
D5503
RB530SM-30T2R-GP-U
LCD_SELF_TEST_ON
D5501
EDP_VDD_EN_R
3D3V_LCDVDD_S5
Non Common part
3D3V_S5
Layout 40 mil
U5501
RT9724GB-GP
74.09724.09F
R5513
100KR2J-1-GP
C5516
SCD1U6D3V1KX-GP
C5517
SC4D7U6D3V3KX-GP
C5518
SCD1U6D3V1KX-GP
3D3V_S0
R5509
1KR2J-1-GP
L_BKLT_CTRL
R5510
33R2J-2-GP
LCD_BRIGHTNESS_R
D5504
RB530SM-30T2R-GP-U
LCD_BRIGHTNESS
D5502
C5524
SC100P50V2JN-L-GP
eDP_AUX_CON_N
R5502
100KR2J-1-GP
eDP_AUX_CON_P
R5503
3D3V_S0_TOUCH
R5511
0R0603-PAD-1-GP-U
C5503
SCD1U25V2KX-GP
C5504
SCD01U50V2KX-1GP
C5505
SCD1U6D3V1KX-GP
LCD Connector
LCD1
eDP_TX_CPU_N1
eDP_TX_CPU_P1
eDP_TX_CPU_N0
eDP_TX_CPU_P0
eDP_AUX_CPU_P
eDP_AUX_CPU_N
TOUCH_USB20_N
TOUCH_USB20_P
TOUCH_STOP#
eDP_HPD_CPU
EPRIVACY_CONTROL
LCD_SELF_TEST_ON
BLON_OUT
BLON_OUT_C
C5531
C5519
C5530
C5521
C5509
C5510
SCD1U6D3V1KX-GP
eDP_TX_CON_N1
eDP_TX_CON_P1
eDP_TX_CON_N0
eDP_TX_CON_P0
eDP_AUX_CON_P
eDP_AUX_CON_N
KYOCERA-CON30-GP
020.K0159.0030
DCBATOUT: Need 1~3 empty-pin from DCBATOUT to the signals or other power net. (Apply to TNB, LNB)
Near LCD1 (LCD)
AFTP5501 TOUCH_STOP#
AFTP5502 LCD_BRIGHTNESS
AFTP5503 BLON_OUT_C
AFTP5504 EPRIVACY_CONTROL
AFTP5505 LCD_SELF_TEST_ON
AFTP5506 3D3V_LCDVDD_S5
AFTP5507 19V_DCBATOUT_LCD
AFTP5508 3D3V_S0_TOUCH
AFTP5509
C5511
SC1U6D3V1MX-GP
C5512
SCD1U6D3V1KX-GP
R5507
1KR2J-1-GP
R5508
100KR2J-1-GP
C5514
SC100P50V2JN-3GP
R5565
10KR2J-3-GP
C5513
R5566
ED5501
AZ5125-02S-R7G-GP
R5512
100KR2J-1-GP
BB1_EVT_MAIN_W031
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W047
BB1_FVT_MAIN_W017
BB1_FVT_MAIN_W023
BB1_SIT_MAIN_W001
BB1_SVT_MAIN_W001
BB1_SVT_MAIN_W008

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DISPLAY (LCD/CAM/TOUCH)

Size A2 | Document Number: Bumblebee-1 | Rev -1

Date: Thursday, May 30, 2019 |

BB1_EVT_MAIN_W013
BB1_EVT_MAIN_W017
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W015
BB1_EVT_MAIN_W017
BB1_SVT_MAIN_W008

TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY1)
L: USB Type-C has higher priority when both ports are plugged H: HDMI Port has higher priority when both ports are plugged

Note: SW is pulled down with 150K-ohm internally

Place 0.1uF *4 and 0.01uF *4 caps near each VDD33 pin of PS8337

H: 4.7K-ohm
M: 150K-ohm
L: DY

WHL DDI

TO PS8747B

HDMI

WHL DDI

I2C SWITCH

Size	Document Number	Rev
A2	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 56 of 99

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDI DEMULTIPLEXER (PS8337B)

BB1_EVT_MAIN_W017
BB1_EVT_MAIN_W024
BB1_EVT_MAIN_W032
BB1_FVT_MAIN_W017
BB1_FVT_MAIN_W028

5V_S0
5V_S0_HDMI
F5701
POLYSW-1D1A6V-10-GP
D5701
TBAW56-GP
HDMI_SDA_CON_R
HDMI_SCL_CON_R
RN5701
SRN2K2J-1-GP

AFTP5701
AFTP5702
AFTP5703
AFTP5704
AFTP5705
HDMI_SCL_CON
HDMI_SDA_CON
HDMI_HPD_CON

HDMI CONN

HDMI1
HDMI (A_Type)
SKT-HDMI23-193-GP-U
022.10025.0321

1	TMDS_DATA2+	GND	20
2	TMDS_DATA2_SHIELD	GND	21
3	TMDS_DATA2-		
4	TMDS_DATA1+		
5	TMDS_DATA1_SHIELD		
6	TMDS_DATA1-		
7	TMDS_DATA0+		
8	TMDS_DATA0_SHIELD		
9	TMDS_DATA0-		
10	TMDS_CLOCK+		
11	TMDS_CLOCK_SHIELD		
12	TMDS_CLOCK-		
13	CEC		
14	RESERVED#14		
15	SCL		
16	SDA		
17	DDC/CEC_GROUNG		
18	+5V_POWER	GND	22
19	HOT_PLUG_DETECT	GND	23

SCD1U6D3V1KX-GP
EC5701

56	HDMI_DDI_TX_CON_P2	ER5701 1 2 180R2F-1-GP
56	HDMI_DDI_TX_CON_N2	
56	HDMI_DDI_TX_CON_P1	ER5702 1 2 180R2F-1-GP
56	HDMI_DDI_TX_CON_N1	
56	HDMI_DDI_TX_CON_P0	ER5703 1 2 180R2F-1-GP
56	HDMI_DDI_TX_CON_N0	
56	HDMI_DDI_TX_CON_P3	ER5704 1 2 180R2F-1-GP
56	HDMI_DDI_TX_CON_N3	
56	HDMI_SCL_CON	
56	HDMI_SDA_CON	
56	HDMI_HPD_CON	

EMC

ED5701
AZ1043-04F-R7G-GP
NEAR HDMI CONN

HDMI_DDI_TX_CON_N3	8,3,1	10	HDMI_DDI_TX_CON_N3
HDMI_DDI_TX_CON_P3	2	9	HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N0	4	7	HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_CON_P0	5	6	HDMI_DDI_TX_CON_P0

EMC

ED5703
AZ1043-04F-R7G-GP
NEAR HDMI CONN

HDMI_HPD_CON	8,3,1	10	HDMI_HPD_CON
HDMI_SCL_CON	2	9	HDMI_SCL_CON
HDMI_SDA_CON	4	7	HDMI_SDA_CON
	5	6	

EMC

ED5702
AZ1043-04F-R7G-GP
NEAR HDMI CONN

HDMI_DDI_TX_CON_N1	8,3,1	10	HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_CON_P1	2	9	HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N2	4	7	HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_CON_P2	5	6	HDMI_DDI_TX_CON_P2

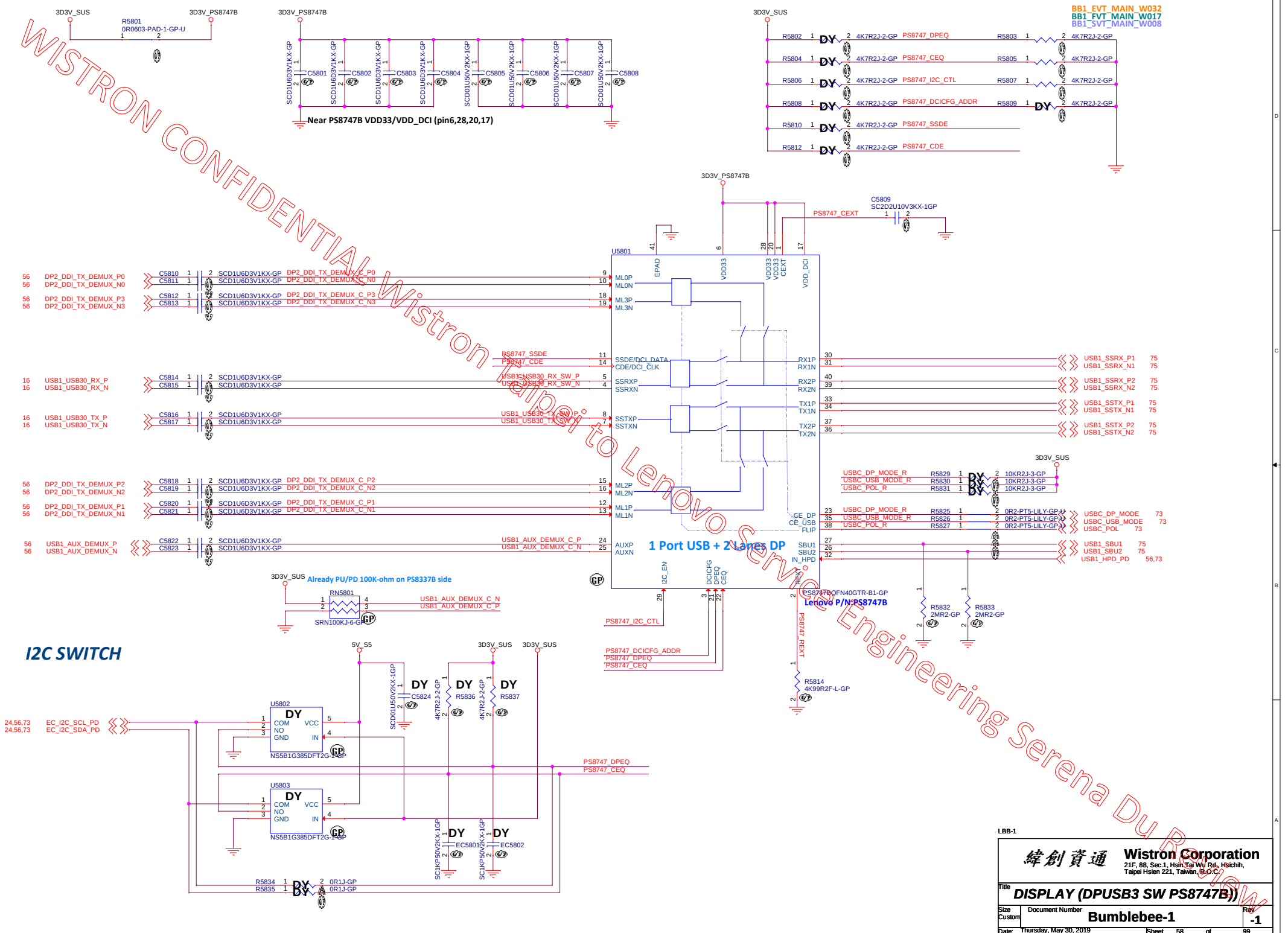
LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISPLAY (HDMI CONN)

Size	Document Number	Rev
A3	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 57 of 99


BB1_EVT_MAIN_W032
BB1_FVT_MAIN_W017
BB1_SVT_MAIN_W008
WISTRON CONFIDENTIAL Wistron Property to Lenovo Service Engineering Serena Du Review
U5801
PS8747BQFN40GTR-B1-GP
Lenovo P/N:PS8747B
1 Port USB + 2 Lanes DP
I2C SWITCH
Near PS8747B VDD33/VDD_DCI (pin6,28,20,17)
Already PU/PD 100K-ohm on PS8337B side
U5802
U5803
NS5B1G385DFT2G-1-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
DISPLAY (DPUSB3 SW PS8747B))
Bumblebee-1
-1
Thursday, May 30, 2019
58
99

BLANK

LBB-1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DISPLAY (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-1**	**-1**

Date: Thursday, May 30, 2019 Sheet 59 of 99

BLANK

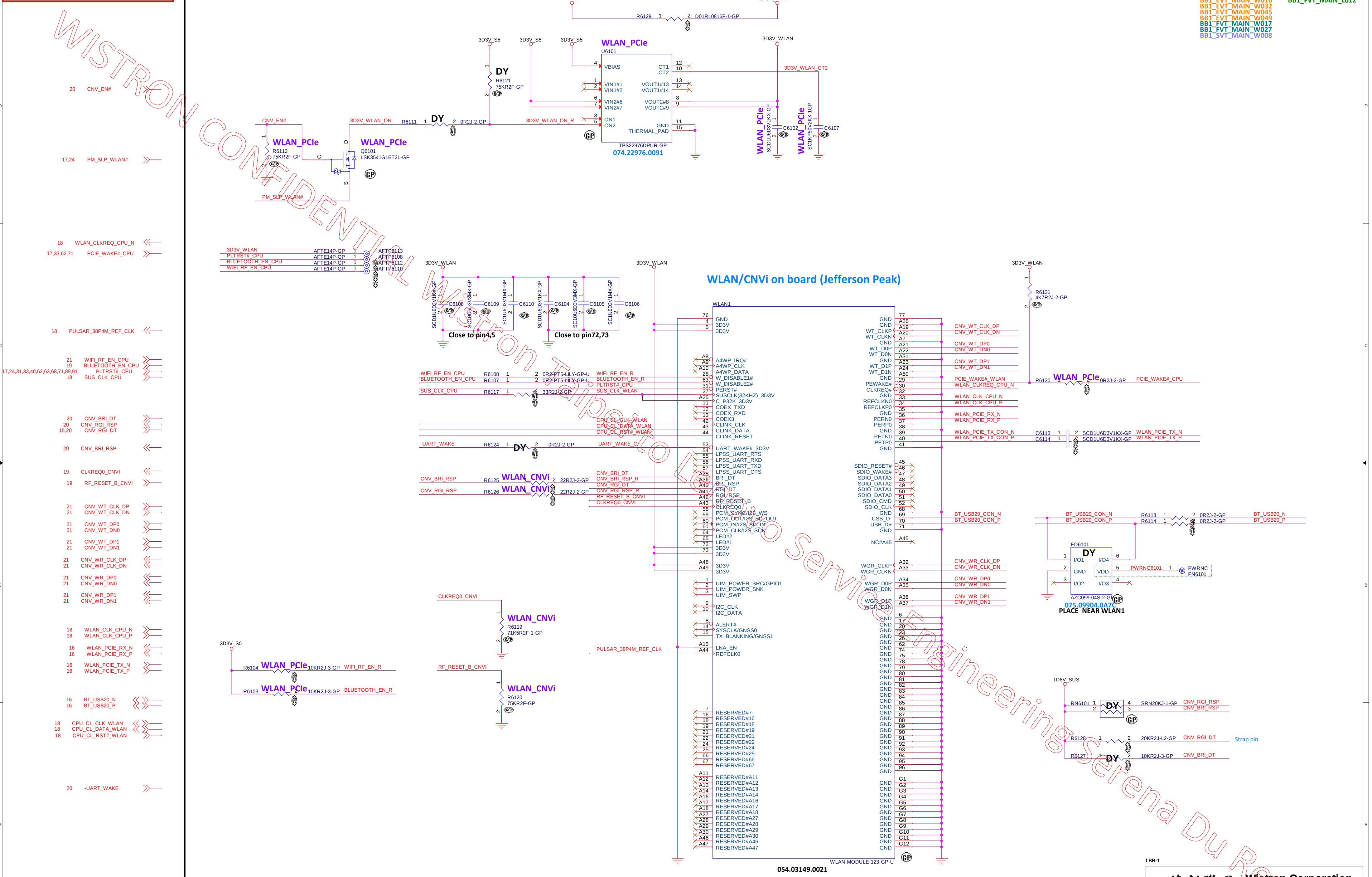
LBB-1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD)*		
Size: A4	Document Number: **Bumblebee-1**	Rev: **-1**
Date: Thursday, May 30, 2019	Sheet 60 of 99	

Main Func = WLAN



BB1_EVT_MAIN_W006
BB1_EVT_MAIN_W016
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W045
BB1_EVT_MAIN_W049
BB1_FVT_MAIN_W017
BB1_FVT_MAIN_W027
BB1_SVT_MAIN_W008
BB1_FVT_MAIN_L005
BB1_FVT_MAIN_L012

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WLAN /CNVi)

Size: A2 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 61 of 99

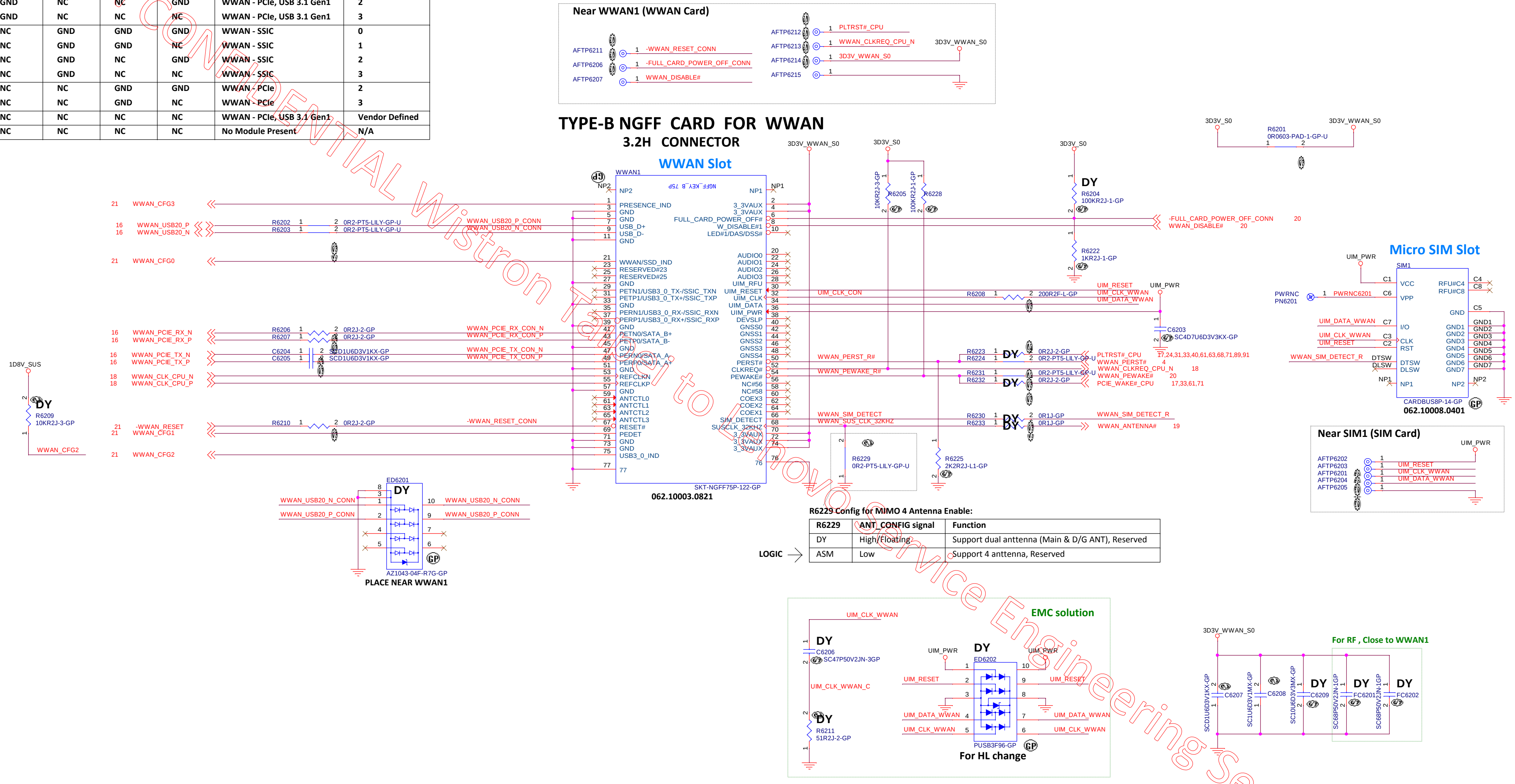
BB1_EVT_MAIN_W008 BB1_FVT_MAIN_L009
BB1_EVT_MAIN_W015 BB1_FVT_MAIN_L010
BB1_EVT_MAIN_W024 BB1_FVT_MAIN_L011
BB1_EVT_MAIN_W032 BB1_SIT_MAIN_L001
BB1_FVT_MAIN_W017
BB1_SVT_MAIN_W008
BB1_SVT_MAIN_W009

TABLE:

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)	Module Type & Main Host Interface	Port Configuration
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined
15	NC	NC	NC	NC	No Module Present	N/A

TABLE:

Module	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)
Fibcom L830-EB	NC	GND	GND	GND
Fibcom L850-GL	GND	NC	GND	GND



R6229 Config for MIMO 4 Antenna Enable:

R6229	ANT_CONFIG signal	Function
DY	High/Floating	Support dual antenna (Main & D/G ANT), Reserved
ASM	Low	Support 4 anttenna, Reserved

LOGIC

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: M.2 SOCKET 2 MODULE I/F

Size: A2 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 62 of 99

TYPE-M M.2 CARD FOR SSD

SSD1 — NGFF_KEY_M 75P — SKT-MINI67P-32-GP

1	GND		2	3VAUX	3D3V_S0_SSD
3	GND		4	3VAUX	
5	PETP3	PETN3	6	NC#6	
7	PETN3	PETP3	8	NC#8	-PLP_INT
9	GND		10	DAS/DSS#	
11	PERN3		12	3VAUX	
13	PERP3		14	3VAUX	
15	GND		16	3VAUX	
17	PETP2	PETN2	18	3VAUX	
19	PETN2	PETP2	20	3VAUX	
21	GND		22	NC#20	
23	PERN2		24	NC#22	
25	PERP2		26	NC#24	
27	GND		28	NC#26	
29	PETN1		30	NC#28	-PLP_FDBK
31	PETP1		32	NC#30	
33	GND		34	NC#32	
35	PERN1		36	NC#34	
37	PERP1		38	NC#36	
39	GND		40	DEVSLP	SSD_DEVSLP 16
41	PETN0/SATA_B+		42	NC#40	
43	PETP0/SATA_B-		44	NC#42	
45	GND		46	NC#44	
47	PERN0/SATA_A-		48	NC#46	
49	PERP0/SATA_A+		50	NC#48	PLTRST#_SSD
51	GND		52	PERST#/NC#50	
53	REFCLKN		54	CLKREQ#/NC#52	
55	REFCLKP		56	PEWAKE#/NC#54	
57	GND		58	NC#56	
67	NC#67		68	NC#58	
69	PEDET(OC_PCIE/GND_SATA)		70	SUSCLK_32KHZ	
71	GND		72	3VAUX	
73	GND		74	3VAUX	
75	GND		76	3VAUX	
77	GND		76	77	
NP1	NP1		NP2	NP2	

24	SSD_DTCT#			
16	SSD_PCIE_RX_N3			
16	SSD_PCIE_RX_P3			
16	SSD_PCIE_TX_N3	C6302	SCD22U10V2KX-1GP	SSD_PCIE_TX_CON_N3
16	SSD_PCIE_TX_P3	C6303	SCD22U10V2KX-1GP	SSD_PCIE_TX_CON_P3
16	SSD_PCIE_RX_N2			
16	SSD_PCIE_RX_P2			
16	SSD_PCIE_TX_N2	C6304	SCD22U10V2KX-1GP	SSD_PCIE_TX_CON_N2
16	SSD_PCIE_TX_P2	C6305	SCD22U10V2KX-1GP	SSD_PCIE_TX_CON_P2
16	SSD_PCIE_RX_N1			
16	SSD_PCIE_RX_P1			
16	SSD_PCIE_TX_N1	C6306	SCD22U10V2KX-1GP	SSD_PCIE_TX_CON_N1
16	SSD_PCIE_TX_P1	C6307	SCD22U10V2KX-1GP	SSD_PCIE_TX_CON_P1
16	SSD_SATA_RX_P			
16	SSD_SATA_RX_N			
16	SSD_SATA_TX_N	C6308	SCD22U10V2KX-1GP	SSD_SATA_TX_CON_N
16	SSD_SATA_TX_P	C6309	SCD22U10V2KX-1GP	SSD_SATA_TX_CON_P
18	SSD_CLK_CPU_N			
18	SSD_CLK_CPU_P			
16	M2_SSD_PEDET			

PEDET (M2_SSD_PEDET)
SATA Device GND
PCIe Device Open

062.10003.0841

3D3V_S0 — SC10U6D3V3MX-GP — C6301 (DY) — F6301 FUSE-3A32V-35-GP — 3D3V_S0 — R6303 10KR2J-3-GP

D6301 RB530SM-30T2R-GP-U (A, K) — PM_PWRBTN# 17,24,99

AFTP6301

R6302 33R2J-2-GP — PLTRST#_CPU 17,24,31,33,40,61,62,68,71,89,91 — SSD_CLKREQ_CPU_N 18

3D3V_S0_SSD — SC10U6D3V3MX-GP — C6310 (DY) — SCD01U50V2KX-1GP — C6311

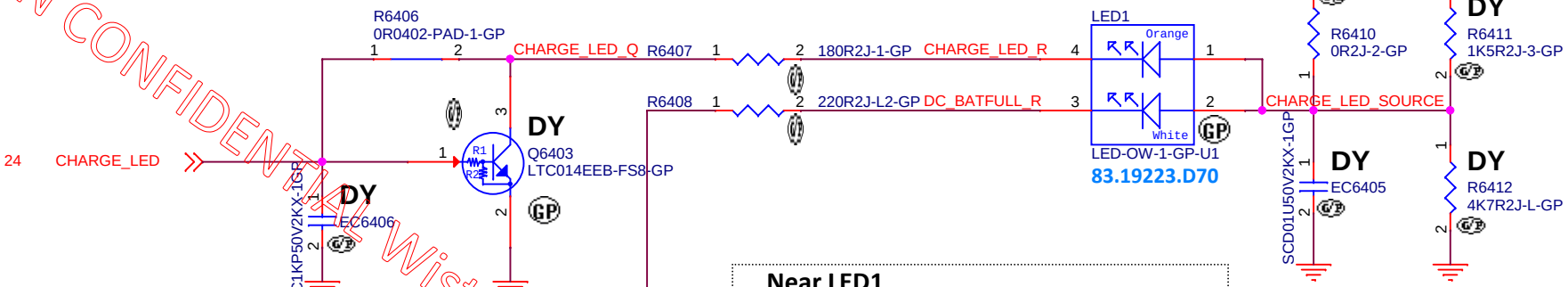
LBB-1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

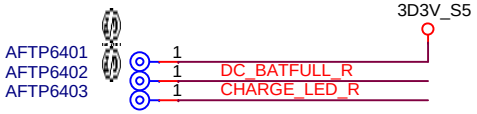
Title: INT IO (SSD M.2)
Size: A3 | Document Number: Bumblebee-1 | Rev: -1
Date: Thursday, May 30, 2019 | Sheet 63 of 99

BB1_EVT_MAIN_W005
BB1_EVT_MAIN_W032
BB1_FVT_MAIN_W017
BB1_SIT_MAIN_W018
BB1_SVT_MAIN_W008
BB1_SVT_MAIN_W010

Dual LED

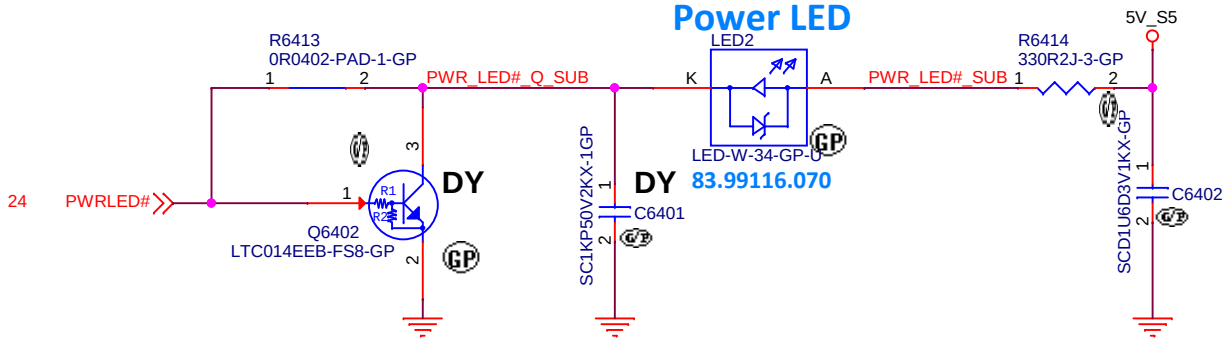


Near LED1



Power Button

Power LED



LBB-1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED/BTN/POWER BTN		
Size: A4	Document Number: Bumblebee-1	Rev: -1
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BB1_EVT_MAIN_W009
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W041
BB1_EVT_MAIN_W010
BB1_EVT_MAIN_W017
BB1_EVT_MAIN_W028
BB1_SIT_MAIN_W010
BB1_SIT_MAIN_W034
BB1_SVT_MAIN_W008

Keyboard Connector

3D3V_S5 5V_S5
R6501 0R0402-PAD-1-GP DY R6502 0R2J-2-GP
C6501 SCD1U6D3V1KX-GP
R6525 20KR2J-L2-GP
The system side only allowed 100ohm resistance for all keyboard LED
R6513 100R2J-2-GP -LED_CAPSLOCK_KB
R6514 100R2J-2-GP -LED_F4_KBD
R6515 100R2J-2-GP -LED_F1_KBD
R6516 100R2J-2-GP -LED_ESC_KBD
3D3V_S5_KBD
EC6501 SCD1U6D3V1KX-GP DY
KB1
JAE-CON36-GP-U
020.K0265.0036

Keyboard Backlight

R6528 4K7R2J-2-GP R6529 4K7R2J-2-GP R6519 10KR2J-3-GP R6524 0R3J-0-U-GP DY R6527 0R0603-PAD-1-GP-0R3J-0-U-GP R6520 DY F6501 POLYSW-1D1A6V-6-GP
KBBL1
JAE-CON12-1-GP-U
20.K0801.012
C6502 SC220P50V2KX-3GP
C6503 SCD01U50V2KX-1GP
C6504 SC4D7U6D3V2MX-GP-U DY

Near KBBL1 (Keyboard Backlight)

AFTP6510 -KBD_BL_DTCT
AFTP6511 KBD_BL_PWM
AFTP6512 5V_S0_LED_R
AFTP6513 TP4_CLK_TPAD
AFTP6514 TP_LEFT
AFTP6515 TP_RIGHT
AFTP6516 TP_MIDDLE
AFTP6517 TP4_RESET
AFTP6518 TP4_DATA_TPAD
AFTP6519 3D3V_S0_TP
AFTP6520

ClickPad Connector

R6526 10KR2J-3-GP R6503 0R0402-PAD-1-GP R6522 4K7R2J-2-GP R6523 4K7R2J-2-GP
R6530 0R2-PT5-LILY-GP-U
TPAD1
KYO-CON12-1-GP
020.K0185.0012

Near KB1 (Keyboard)

AFTP6501 TP_MIDDLE
AFTP6502 TP_RIGHT
AFTP6503 TP_LEFT
AFTP6504 -LED_CAPSLOCK_KB
AFTP6505 -HOTKEY
AFTP6506 -LED_F4_KBD
AFTP6530 -LED_F1_KBD
AFTP6507 -LED_ESC_KBD
AFTP6508 3D3V_S5_KBD
AFTP6509

Near TPAD1 (ClickPad)

AFTP6529 PAD_DISABLE
AFTP6521 IPD_DATA_TPAD
AFTP6522 IPD_CLK_TPAD
AFTP6523 PAD_RESET#
AFTP6524 3D3V_S0_CP_R
AFTP6525 TP_SMB_SDA
AFTP6526 TP4_CLK_TPAD
AFTP6527 TP4_DATA_TPAD
AFTP6531 TP_SMB_SCL
AFTP6528

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (KB/CP/TP)
Size: A3 | Document Number: Bumblebee-1 | Rev: -1
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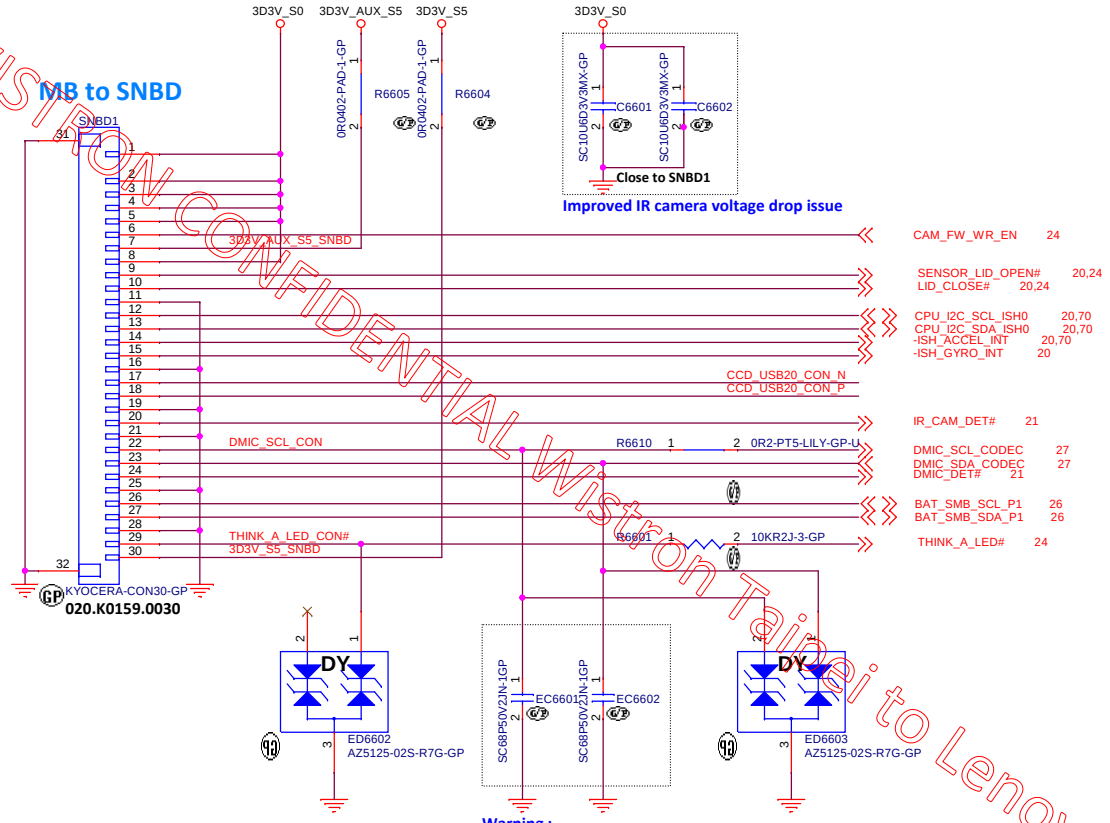
BB1_EVT_MAIN_W014
BB1_EVT_MAIN_W024
BB1_SIT_MAIN_W003
BB1_SIT_MAIN_W018
BB1_SIT_MAIN_W027
BB1_SIT_MAIN_W029
BB1_SIT_MAIN_W030
BB1_SIT_MAIN_W031
BB1_SIT_MAIN_W033
BB1_SVT_MAIN_W008

BB1_EVT_MAIN_L013

MB to SNBD

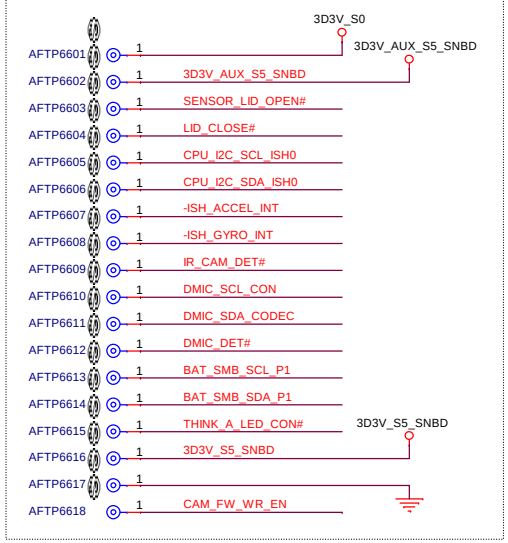


Camera

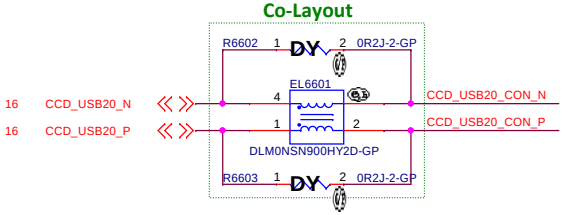
P-Sensor

Warning :
Please do MIC related test before changing Cap Value

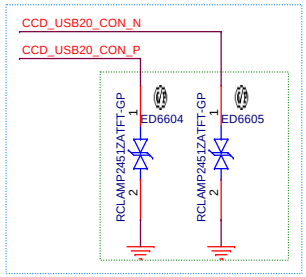
Near SNBD1 (Sensor board)



Co-Layout



LBB-1 Layout impact:
WWAN antenna interference, change to small size



For CAMERA ESD failed solution

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO BOARD CONN

Size: A3 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 66 of 99

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LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SENNSOR (HALL SENSOR)

Size	Document Number	Rev
A4	Bumblebee-1	-1

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Main Func = Debug

18,24 LPC_SERIRQ_CPU
18 LPC_CLK_DB
17,24,31,33,40,61,62,63,71,89,91 PLTRST#_CPU
18,24 LPC_FRAME#_CPU
18,24 LPC_AD_CPU_P3
18,24 LPC_AD_CPU_P2
18,24 LPC_AD_CPU_P1
18,24 LPC_AD_CPU_P0
24 EC_E51_TXD
24 EC_E51_RXD
21 CPU_UARTx_TXD
21 CPU_UARTx_RXD

3D3V_S0
3D3V_S0
49K9R2F-L-GP
LPC R6801
49K9R2F-L-GP
LPC R6802

LPC Connector

LPC DBG1
ZZ.F0765.0141
ACES-CON14-5-GP
20.F0765.014

LPC_SERIRQ_CPU
LPC_CLK_DB
PLTRST#_CPU
LPC_FRAME#_CPU
LPC_AD_CPU_P3
LPC_AD_CPU_P2
LPC_AD_CPU_P1
LPC_AD_CPU_P0
EC_E51_TXD
EC_E51_RXD
CPU_UARTx_TXD
CPU_UARTx_RXD

LBB-1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DEBUG (LPC DEBUG)
Size: A4
Document Number: Bumblebee-1
Rev: -1
Date: Thursday, May 30, 2019
Sheet 68 of 99

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LBB-1

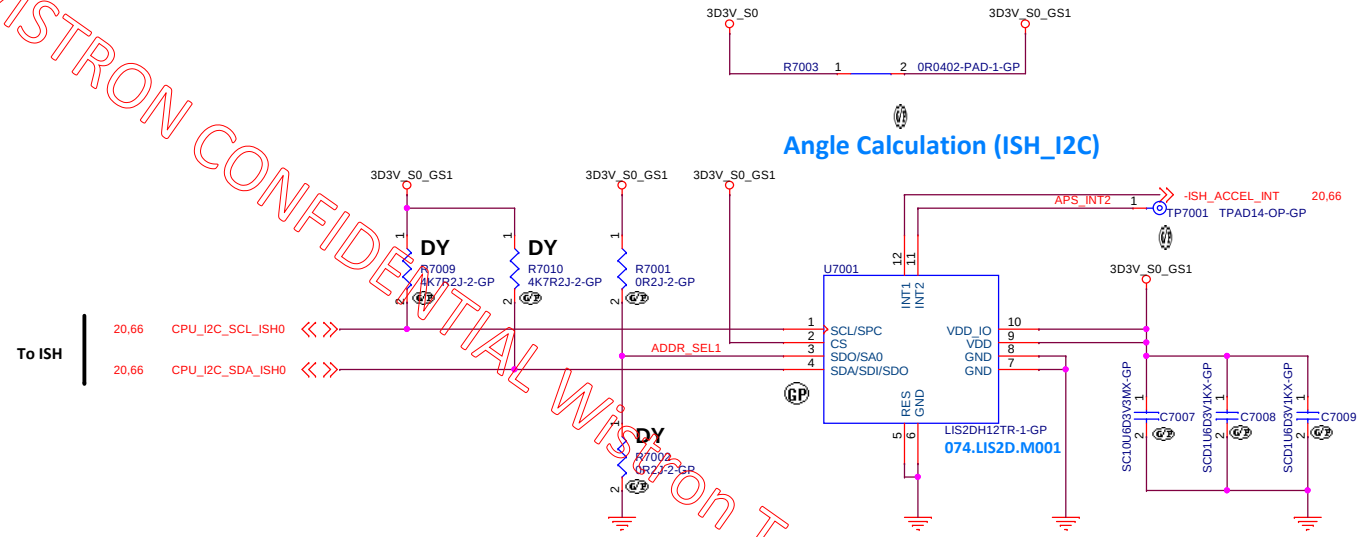
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SENSOR (RSVD)

Size	Document Number	Rev
A4	Bumblebee-1	-1

Date: Thursday, May 30, 2019 Sheet 69 of 99

BB1_EVT_MAIN_W032
BB1_FVT_MAIN_W012
BB1_FVT_MAIN_W017
BB1_FVT_MAIN_W032
BB1_SVT_MAIN_W008



TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

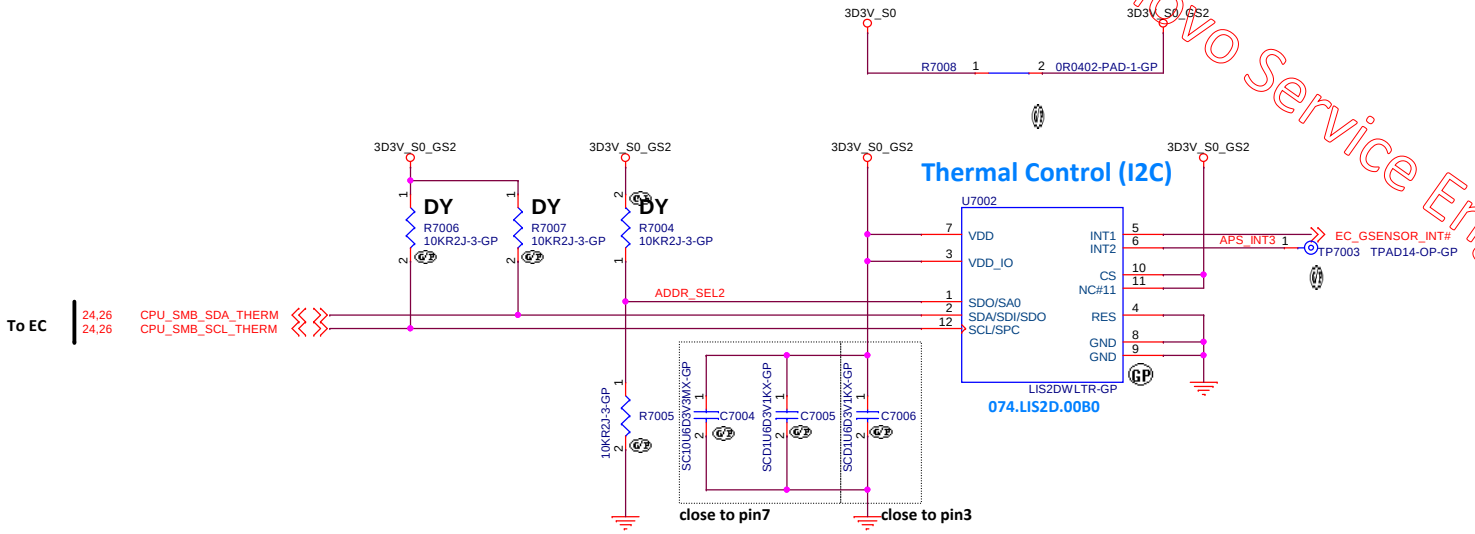
TABLE for Angle Detection (U7001): Tri-axis Digital Accelerometer

P/N	ADDR_SEL1	Address
LIS2DH12TR	H	32h(W) & 33h(R)
	L	30h(W) & 31h(R)

← Logic

TABLE of G-Sensor (U7001)

Vendor	P/N	Wistron P/N
ST	LIS2DH12TR	074.LIS2D.M001



TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

TABLE for Angle Detection (U7002): Tri-axis Digital Accelerometer

P/N	ADDR_SEL2	Address
LIS2DWLTR	H	32h(W) & 33h(R)
	L	30h(W) & 31h(R)
KX022-1020	H	3Eh(W) & 3Fh(R)
	L	30Ch(W) & 3Dh(R)

← Logic

TABLE of G-Sensor(U7002)

Vendor	P/N	Wistron P/N
ST	LIS2DWLR	074.LIS2D.00B0
KIONIX	KX022-1020	074.00022.00B0

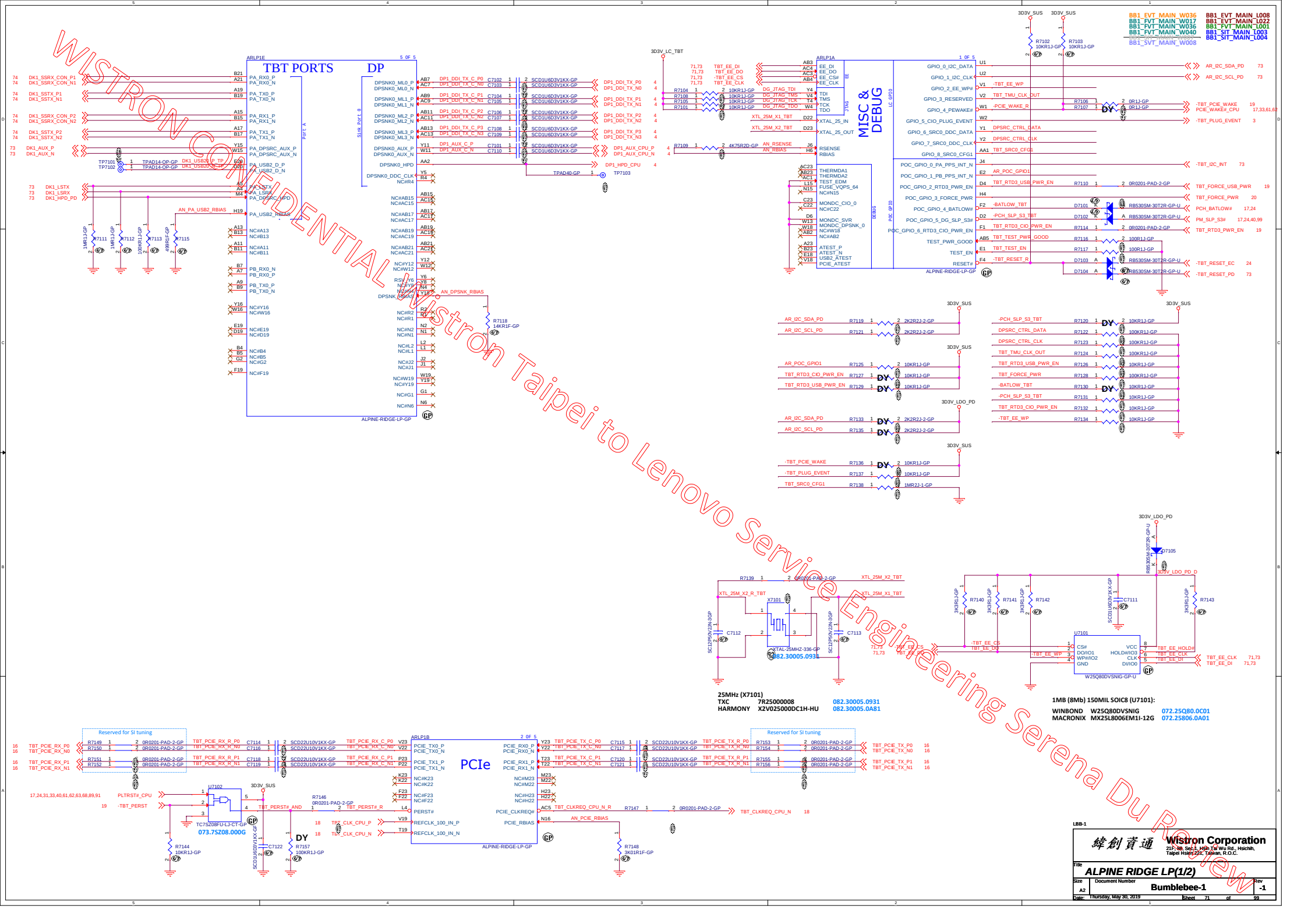
LBB-1

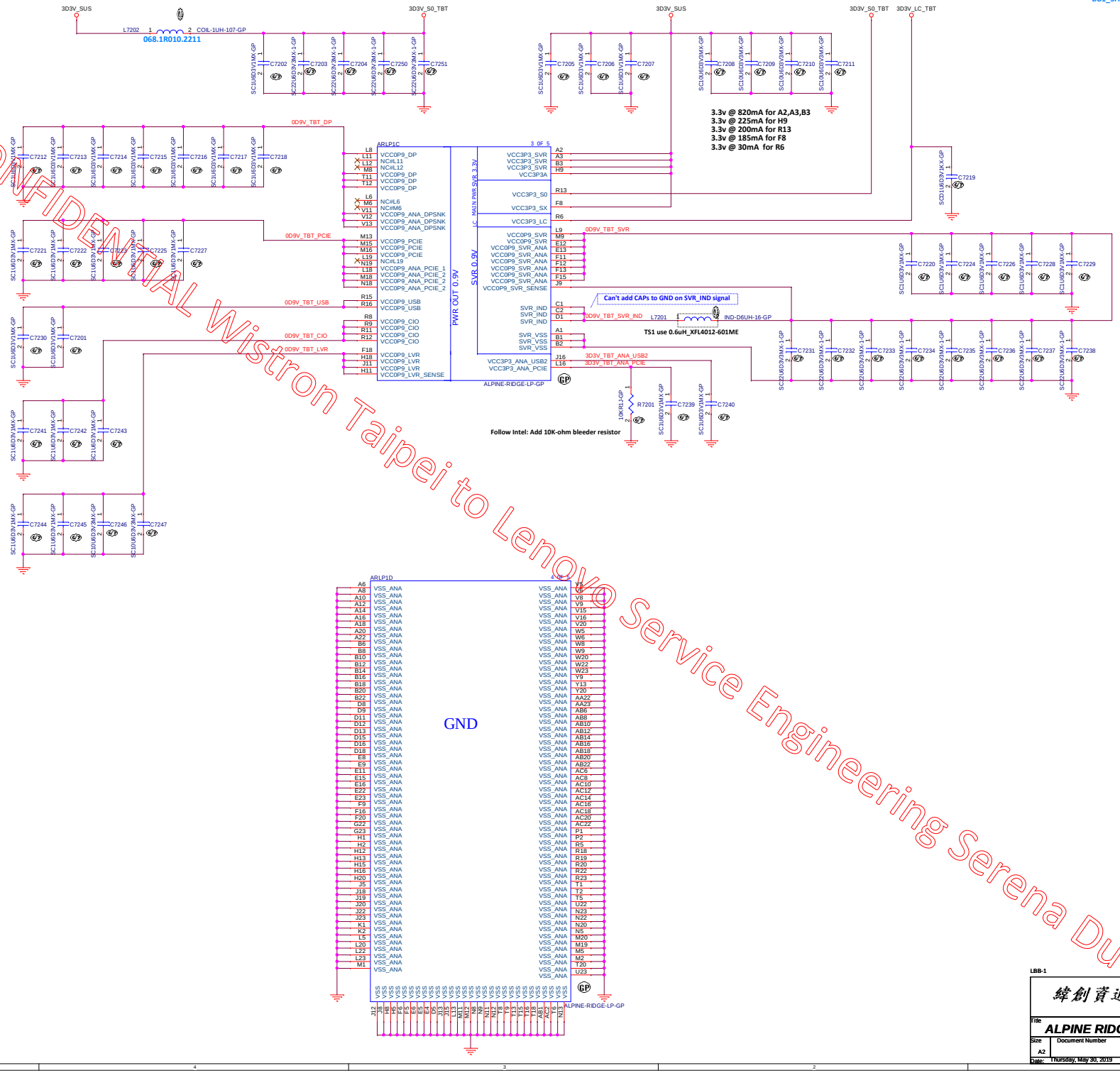
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SENSOR (G-SENSOR)

Size: A3 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 70 of 99





Wistron Corporation			
Title	ALPINE RIDGE LP(2/2)		
Size	Document Number		Rev
A2	Bumblebee-1		-1
Date: Thursday, May 30, 2019	Sheet 72 of 99		

TABLE BUSPOWER Configuration (PD_ADCIN1 Resister Divider)

DIV = R7301 / (R7303 + R7301)		Configuration
DIV MIN	DIV MAX	
0.00	0.18	BP_NoRespones
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

LOGIC

DIV = R2 / (R1 + R2)

TABLE I2C Addrssing (TBD)

I2C1 (to EC)	TBT PORT	0X23
	USBC PORT	0X27
I2C2 (to AR)	TBT PORT	0X38
	USBC PORT	0X3F

D7301, D7302
ONSEMI NSR20F30NXT5G 083.20F30.008H
VISHAY VSKY20301608 083.20301.008F

PLACE NEAR U7301

(Split-pad)
SN1701012RJTR(SL80Q56940AA)
TPS65988CE RJTR Symbol

(with split-pad)
SN1701012 is equivalent device of TPS65988
U7301 will use BOM control by co-lay symbol issue

TS3DS10224 is used for:
(1) Multiplexing DP_AUX signal and TBT_LS signal (TBTx_DP/TBT_MODE)
(2) Supporting cable flip (TBTx_POL)
Those function had been supported in TPS65982 but not in TPS65988/SN1701012

LBB-1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (TYPEC PD TPS65988)

Size: A2 | Document Number: Bumblebee-1 | Rev: -1

Date: Thursday, May 30, 2019 | Sheet 73 of 99

FPF2281 will be change to other parts due to not match current limit.

BB1_EVT_MAIN_W030
BB1_EVT_MAIN_W032
BB1_FVT_MAIN_W006
BB1_FVT_MAIN_W017
BB1_FVT_MAIN_W018
BB1_FVT_MAIN_W019
BB1_FVT_MAIN_W031
BB1_SVT_MAIN_W008
BB1_SVT_MAIN_W013
BB1_EVT_MAIN_L022
BB1_FVT_MAIN_L003

CC PROTECTION

U7403 SN1710033RUKR-1-GP
074.17100.0073

The VBIAS pin requires a minimum 35-VDC rated capacitor, and a 50-VDC rated capacitor is recommended.

VOLTAGE MONITOR

U7401 FPF2281BUCX-F130-1-GP
074.02281.M001

LAN ISN Test Related

Over Voltage Lock Out Trip Threshold = 1.20 * (1 + R7401 / R7402)

DY
Anti-Surge Resistor (R7403):
KOA SG73P1JTTD101J 063.1013F.015V
ROHM ESR03EZPJ101 063.10132.015V

DY
Q7401:
ONSEMI (FAIRCHILD) 2N7002KW 084.27002.0A3K
NXP NX7002BKW 084.07002.0A3K

Co-lay with U7402 USB SW

U7402 TS3USB31ERSER-GP

U7402 TABLE

Vendor	Vendor PN	Wistron PN
TI	TS3USB31E	073.00331.0003
ONSemi	NLAS7213MUTBG	073.07213.0003

TS3USB31E is placed for security reason.
When unknown USB Type-C power adapter is attached, utility in OS shuts down USB 2.0 signal from USB Type-C port to avoid computer virus.

Place on BOTTOM side

(Support Thunderbolt 3) DOCKING CONN

SCA0N88351AA

ED7401,ED7404,ED7406,ED7408,ED7409,ED7410,ED7411,ED7413

(CDE Test Failed)	INFINEON	ESD101-B1-02ELS	083.00101.00AF
(CDE Test Failed)	LITTELFUSE	SESD0201X1BN-0015-096	083.00201.08AF
(CDE Test Passed)	NXP	PESD5V0H1BSFYL	083.5V0H1.00AF
	SEMTECH	RCLAMP3391CTFT	075.03391.0077

ED7402,ED7403,ED7405,ED7407,ED7412,ED7414

SEMTECH	RClamp2451ZA (working voltage = 24V)	083.02451.00A0

Co-Layout

EMC

AZC099-04S-2-GP

VDD pin keep NC

EMC

AZC099-04S-2-GP

VDD pin keep NC

LBB-1

Wistron Corporation
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Title: EXT IO (DOCKING CS18 CONN)
Size: A2
Document Number: Bumblebee-1
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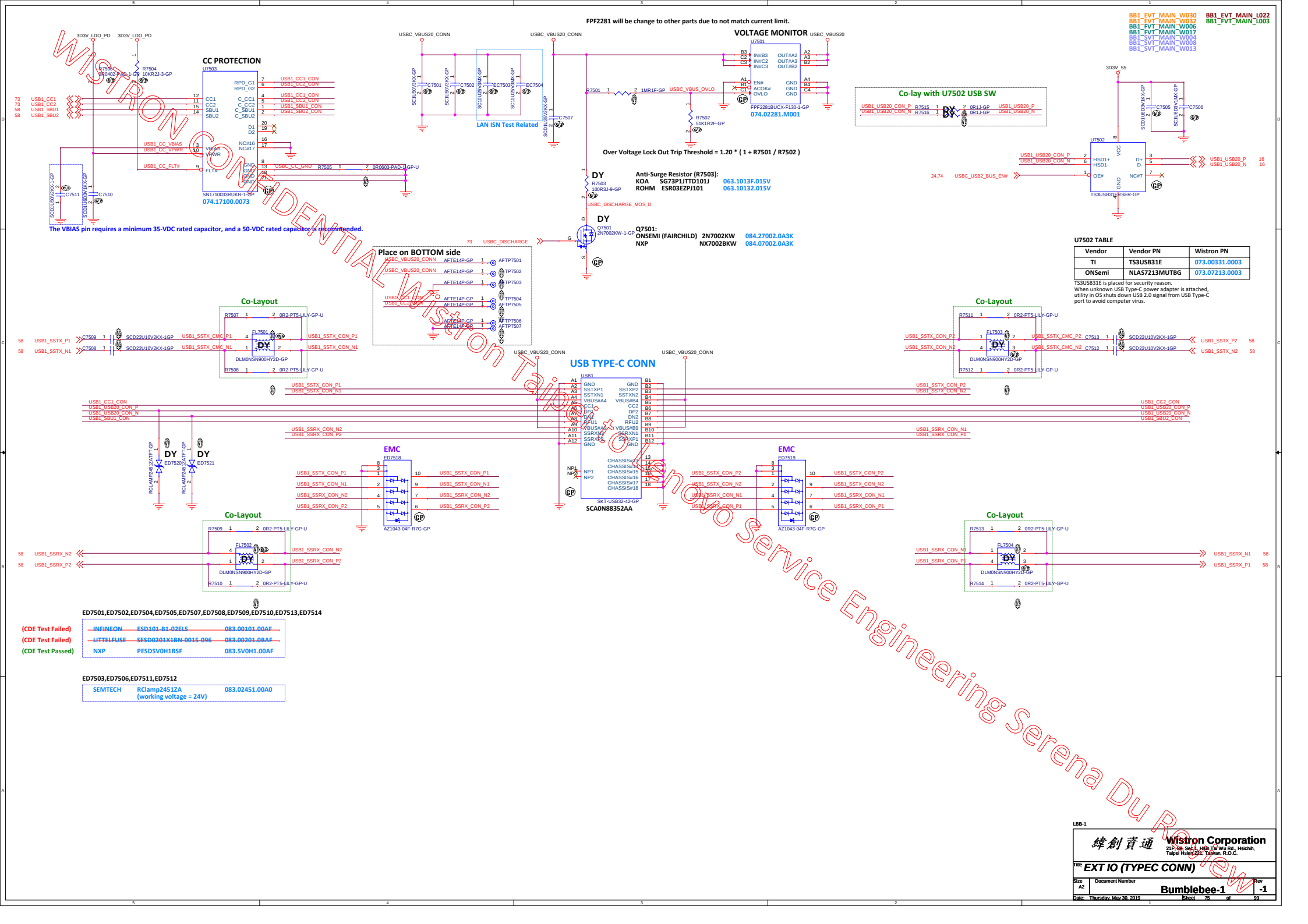
FPF2281 will be change to other parts due to not match current limit.
BB1_EVT_MAIN_W030
BB1_EVT_MAIN_W032
BB1_FVT_MAIN_W006
BB1_FVT_MAIN_W017
BB1_SVT_MAIN_W004
BB1_SVT_MAIN_W008
BB1_SVT_MAIN_W013
BB1_EVT_MAIN_L022
BB1_FVT_MAIN_L003
CC PROTECTION
VOLTAGE MONITOR
Co-lay with U7502 USB SW
Over Voltage Lock Out Trip Threshold = 1.20 * (1 + R7501 / R7502)
Anti-Surge Resistor (R7503):
KOA SG73P1JTTD101J 063.1013F.015V
ROHM ESR03EZPJ101 063.10132.015V
Q7501:
ONSEMI (FAIRCHILD) 2N7002KW 084.27002.0A3K
NXP NX7002BKW 084.07002.0A3K
The VBIAS pin requires a minimum 35-VDC rated capacitor, and a 50-VDC rated capacitor is recommended.
LAN ISN Test Related
Place on BOTTOM side
Co-Layout
USB TYPE-C CONN
SKT-USB32-42-GP
SCA0N88352AA
EMC
U7502 TABLE
Vendor | Vendor PN | Wistron PN
TI | TS3USB31E | 073.00331.0003
ONSemi | NLAS7213MUTBG | 073.07213.0003
TS3USB31E is placed for security reason.
When unknown USB Type-C power adapter is attached, utility in OS shuts down USB 2.0 signal from USB Type-C port to avoid computer virus.
ED7501,ED7502,ED7504,ED7505,ED7507,ED7508,ED7509,ED7510,ED7513,ED7514
(CDE Test Failed) INFINEON ESD101-B1-02ELS 083.00101.00AF
(CDE Test Failed) LITTELFUSE SESD0201X1BN-0015-096 083.00201.08AF
(CDE Test Passed) NXP PESD5V0H1BSF 083.5V0H1.00AF
ED7503,ED7506,ED7511,ED7512
SEMTECH RClamp2451ZA (working voltage = 24V) 083.02451.00A0
Wistron CONFIDENTIAL Wistron Taipei Confidential
Service Engineering Serena Du Review
LBB-1
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title EXT IO (TYPEC CONN)
Size A2 Document Number Bumblebee-1 Rev -1
Date: Thursday, May 30, 2019 Sheet 75 of 99

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)		
Size: A4	Document Number: Bumblebee-1	Rev: -1
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)		
Size: A4	Document Number: Bumblebee-1	Rev: -1
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Title: GPU (RSVD)		
Size: A4	Document Number: Bumblebee-1	Rev: -1
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Title: GPU (RSVD)		
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Title: GPU (RSVD)		
Size: A4	Document Number: Bumblebee-1	Rev: -1
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (RSVD)*		
Size: A4	Document Number: **Bumblebee-1**	Rev: **-1**
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)		
Size: A4	Document Number: Bumblebee-1	Rev: -1
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)		
Size: A4	Document Number: Bumblebee-1	Rev: -1
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU (RSVD)**

Size	Document Number	Rev
A4	**Bumblebee-1**	**-1**

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU (RSVD)**

Size	Document Number	Rev
A4	**Bumblebee-1**	**-1**

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緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU (RSVD)**

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Screw Pad

H1 HOLET237B414X278R103-S1 — Special GND HOLE for Layout
H3 HOLE237R103-GP — ZZ.00PAD.EJ1
H4 HOLE237R103-GP — ZZ.00PAD.EJ1
H5 HOLE217R103-GP — ZZ.00PAD.AI1
H6 HOLE217R103-GP — ZZ.00PAD.AI1
H9 HOLET233B158R142-GP — ZZ.00PAD.VK1
H10 HOLET233B158R142-GP — ZZ.00PAD.VK1
H11 HOLET233B158R142-GP — ZZ.00PAD.VK1
H12 HOLET233B158R142-GP — ZZ.00PAD.VK1

Stand Off

H20 STFT236B142R128H43-3-GP — 34.4LY01.101
H21 STFT237B142R113H47-GP — 434.0DA01.0001
H14 STFT237B142R113H47-GP — 434.0DA01.0001
H15 STFT237B142R113H47-GP — 434.0DA01.0001

Spring Plate

SPR1 SPRING-31-GP-U — 34.49U24.001
SPR2 SPRING-64-GP — 34.4H602.001

Laser QR Code

BB1_EVT_MAIN_W020
BB1_EVT_MAIN_W025
BB1_EVT_MAIN_W027
BB1_EVT_MAIN_W029
BB1_EVT_MAIN_W031
BB1_EVT_MAIN_W048
BB1_EVT_MAIN_W051
BB1_EVT_MAIN_W025
BB1_EVT_MAIN_W026
BB1_EVT_MAIN_W043
BB1_SIT_MAIN_W005
BB1_SIT_MAIN_W011
BB1_SIT_MAIN_W016
BB1_SIT_MAIN_W021
BB1_SIT_MAIN_W023
BB1_SVT_MAIN_W006
BB1_SVT_MAIN_W014

Special GND HOLE for Layout

HL1 HOLET475X368B453X362R119-2P-S1
HL2 HOLET583X414B544X317R119-2P-S
HL3 HOLET662X365B512X329R103-2P-S2
HL4 HOLE315R193
HL5 HOLET315B335X355R119-S
HL6 HOLET237B103R79

Test Point

Place on top side
TP8901 TPAD60 — KBC_PWRBTN# 24,64,74,89

Place on bottom side
TP8902 TPAD60 — KBC_PWRBTN# 24,64,74,89

AFTP8918 AFTE14P-GP — PLTRST#_CPU 17,24,31,33,40,61,62,63,68,71,91
AFTP8921 AFTE14P-GP — KBC_PWRBTN# 24,64,74,89

Place on top side
5V_S5 5V_S0 3D3V_S5 3D3V_S0
AFTP8901 AFTP8912 AFTP8902 AFTP8903 AFTP8904 AFTP8905 AFTP8906 AFTP8907 AFTP8908 AFTP8909 AFTP8910 AFTP8911 — AFTE14P-GP
PLTRST#_EC 24

RF CAPs

19V_DCBATOUT — TOP side — DY — FC8901 FC8902 FC8903 FC8904 FC8905 FC8906 FC8907 FC8908 FC8909 FC8910 FC8911 FC8912 FC8913
1D2V_S3 — TOP side — DY — FC8914 FC8915 FC8916 FC8917 FC8918 FC8919
1V_VCCGT — TOP side / BOTTOM side — DY — FC8920 FC8921
PWR_1D2V — TOP side — DY — FC8923 FC8924
0D9V_LAN — TOP side — DY — FC8925 FC8926
3D3V_WLAN — TOP side — DY — FC8927 FC8928
1D05V_SUS — TOP side / BOTTOM side — DY — FC8929 FC8930
1V_CPU_CORE — TOP side / BOTTOM side — DY — FC8931 FC8932 FC8945 FC8946
19V_DCBATOUT_LCD_R — BOTTOM side — DY — FC8933 FC8934
3D3V_SUS — BOTTOM side — DY — FC8935 FC8936
3D3V_PS8747B — BOTTOM side — DY — FC8937 FC8938
19V_DCBATOUT_LCD — BOTTOM side — DY — FC8939
5V_S0 PWR_DCBATOUT_VDDQ — FC8947 FC8948 FC8949
2D5V_S3 — FC8950
1D2V_S3 — FC8951 FC8952
1D05V_VCCST — FC8953
1V_VCCSA — FC8954
1D05V_VCCIO — FC8956
19V_DCBATOUT — FC8957 FC8958 FC8959 FC8960
PWR_DCBATOUT_VCCSA 5V_S5 — FC8961 FC8962
PWR_DCBATOUT_VCOREA PWR_DCBATOUT_VDDQ — FC8963 FC8964 FC8965
5V_S5 3D3V_PEN_S0 — FC8966 FC8967

EMI CAPs

VINT20_IN — DY — FC8901
BT+_IN1 — DY — FC8902 — Closed to BATT1
VINT20_IN_R 19V_DCBATOUT — DY — FC8903 FC8904
PWR_DCBATOUT_5V PWR_DCBATOUT_3D3V — DY — FC8905 FC8906
PWR_DCBATOUT_VCOREA PWR_DCBATOUT_VCOREB — DY — FC8907 FC8908 — Closed to PU4701 / Closed to PU4702
EC_THINKA_PWRLED 24 — FC8909

LBB-1
緯創資通 Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: UNUSED PARTS (ME/RF/EMI)
Size: A2 | Document Number: Bumblebee-1 | Rev: -1
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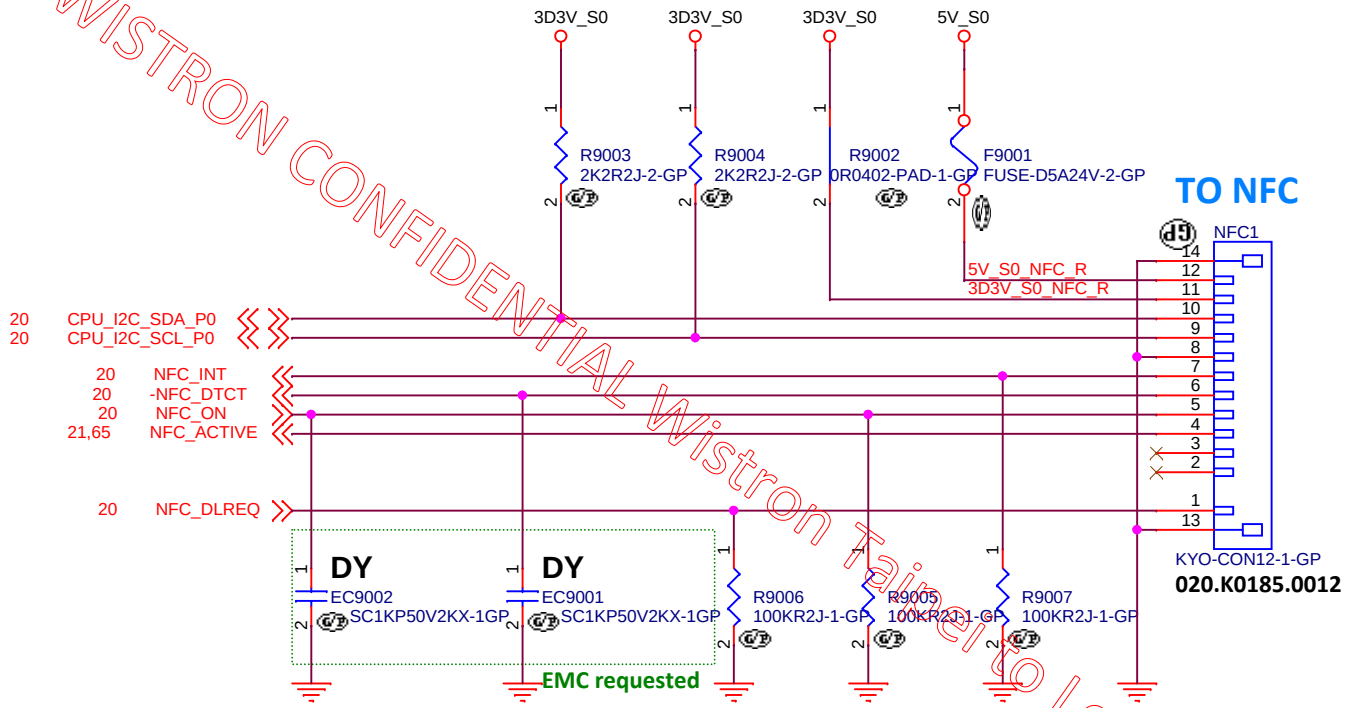

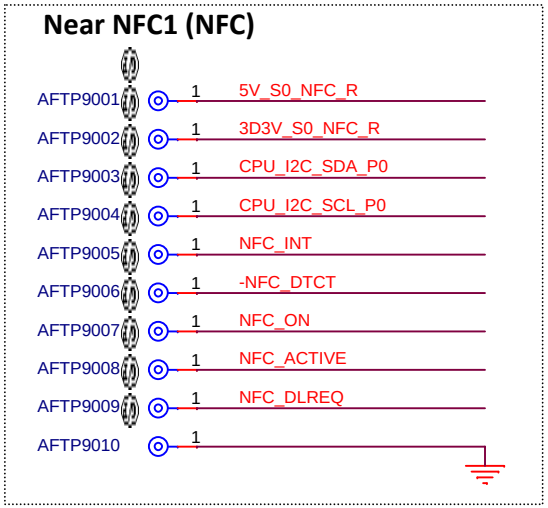

Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C _SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

Remark: P – power supply, G – ground, I – input, O – output, I/O – input/output

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Title: ***INT IO (NFC)***

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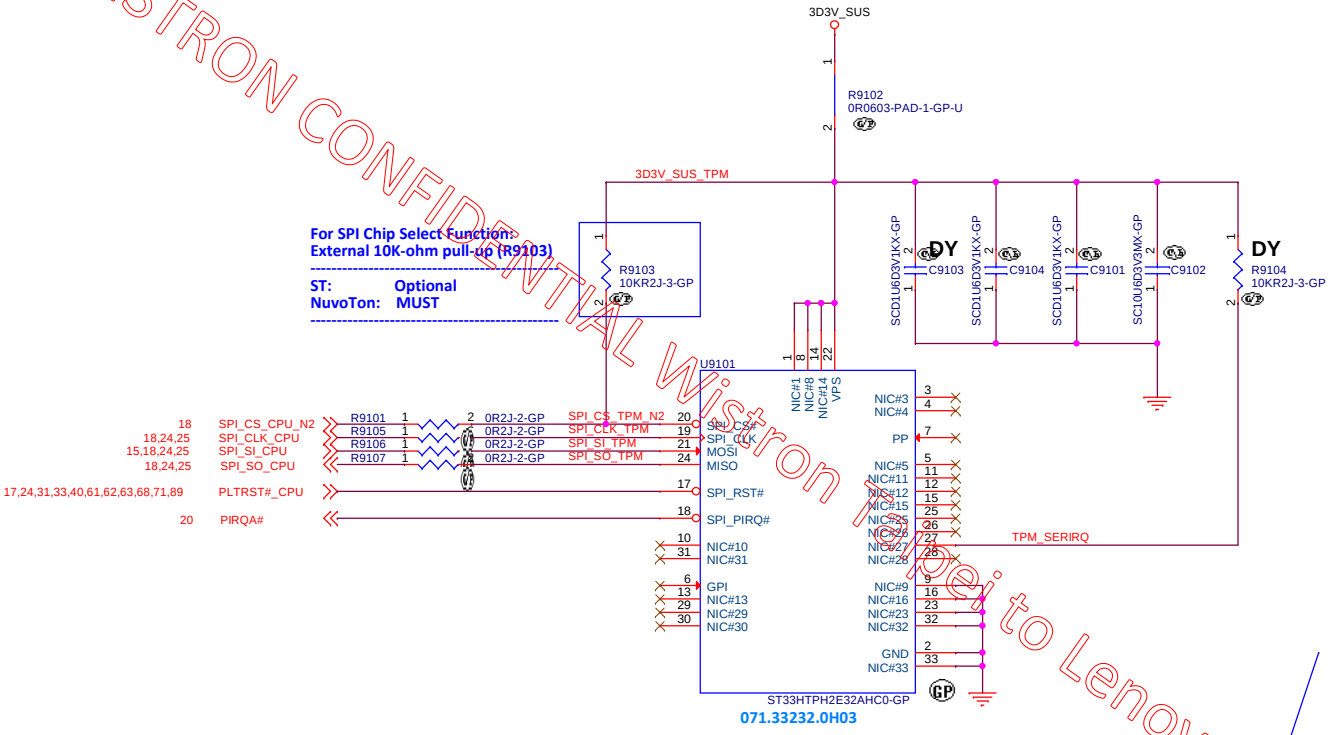
BB1_EVT_MAIN_W032
BB1_EVT_MAIN_W039
BB1_EVT_MAIN_W005
BB1_EVT_MAIN_W017
BB1_SVT_MAIN_W008



TABLE

	EVT		FVT and beyond	
1st	ST33HTPH2E32AHB4	071.33232.0G03	ST33HTPH2E32AHC0	071.33232.0H03
2nd	NPCT750LAAYX	071.00750.0A03	NPCT750LABYX	071.00750.0D03

TABLE

Pin No	TCG PTP Spec(V38)	NuvoTon NPCT750LABYX 071.00750.0D03	ST Micro ST33HTPH2E32AHC0 071.33232.0H03	~~071.09670.0I03~~ Infineon SLB9670VQ2.0 FW7.63
1	VDD	VSB	NC	VDD
2	GND	NC	GND	GND
3	NC	NC	NC	NC
4	GPIO	GPIO/PP	PP	NC
5	NC	NC	NC	NC
6	GPIO	GPIO3	NC	GPIO
7	GPIO	NC	GPIO	PP
8	VDD	VHIO	NC	VDD
9	NC	NC	NC	GND
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	GPIO4	NC	NC
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	GND	NC	NC
17	SPI_RST#	RST#	SPI_RST#	RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#	PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#	CS#
21	MOSI	MOSI/GPIO7	MOSI	MOSI
22	VDD	VHIO	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO0	NC	NC
30	SDA/GPIO0	SCL/GPIO1	NC	NC
31	NC	NC	NC	NC
32	NC	NC	NC	GND

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Title: INT IO (TPM 2.0)

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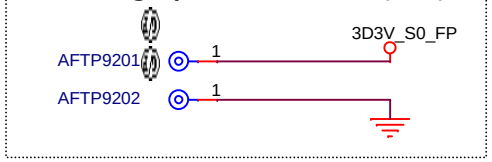
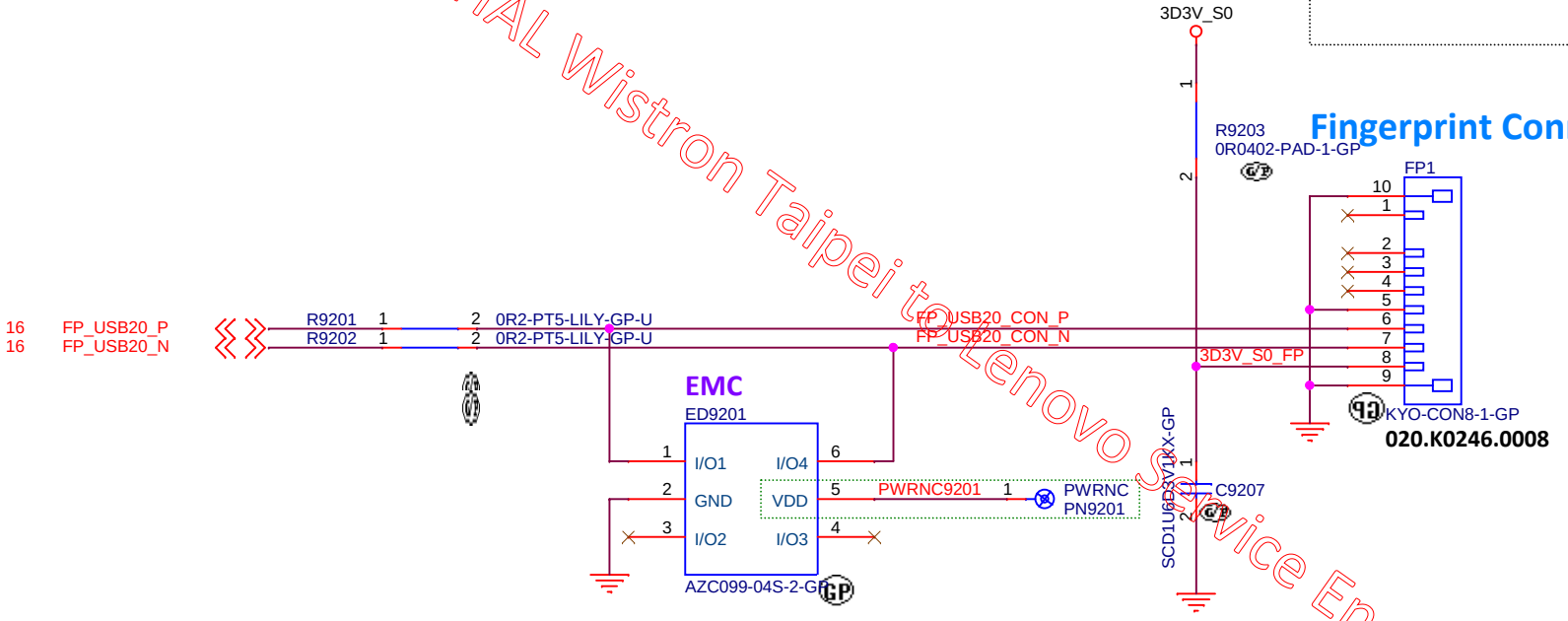
BB1_EVT_MAIN_W032
BB1_FVT_MAIN_W017
BB1_SVT_MAIN_W008

Near Fingerprint Connector (FP1)



Fingerprint Connector



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Title: *INT IO (FINGERPRINT)*		
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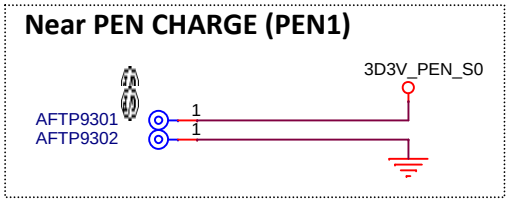

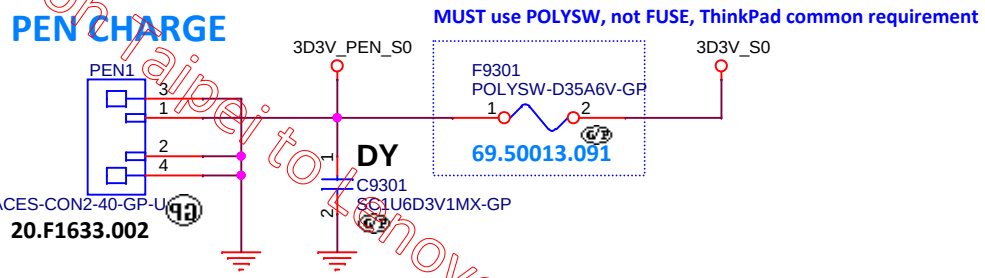

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Title: EXT IO (ACTIVE PEN)		
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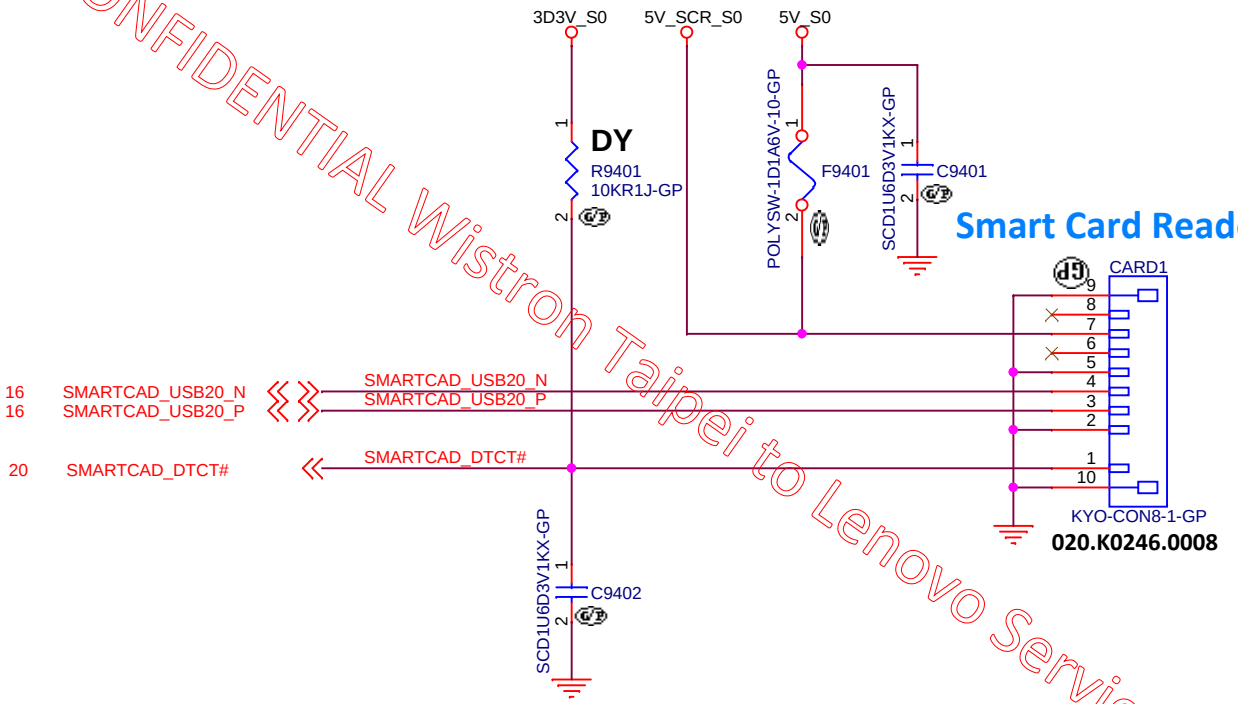
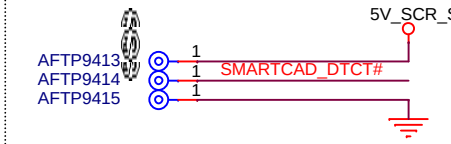
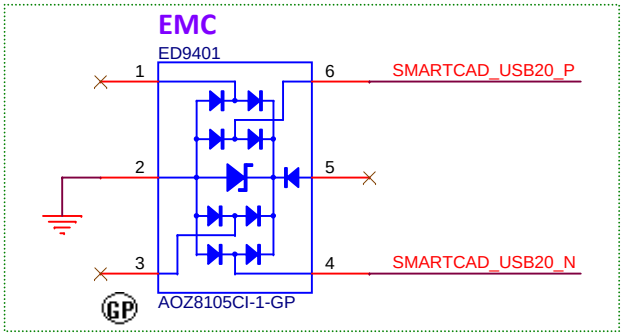
Smart Card Reader CONN



Near Smart Card Reader CONN (CARD1)



EMC



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Title: *EXT IO (SMART CARD)*		
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Title: **EXT IO (RSVD)**

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Title: COMMERCIAL (RSVD)

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Title: COMMERCIAL (RSVD)

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Title
COMMERCIAL (RSVD)

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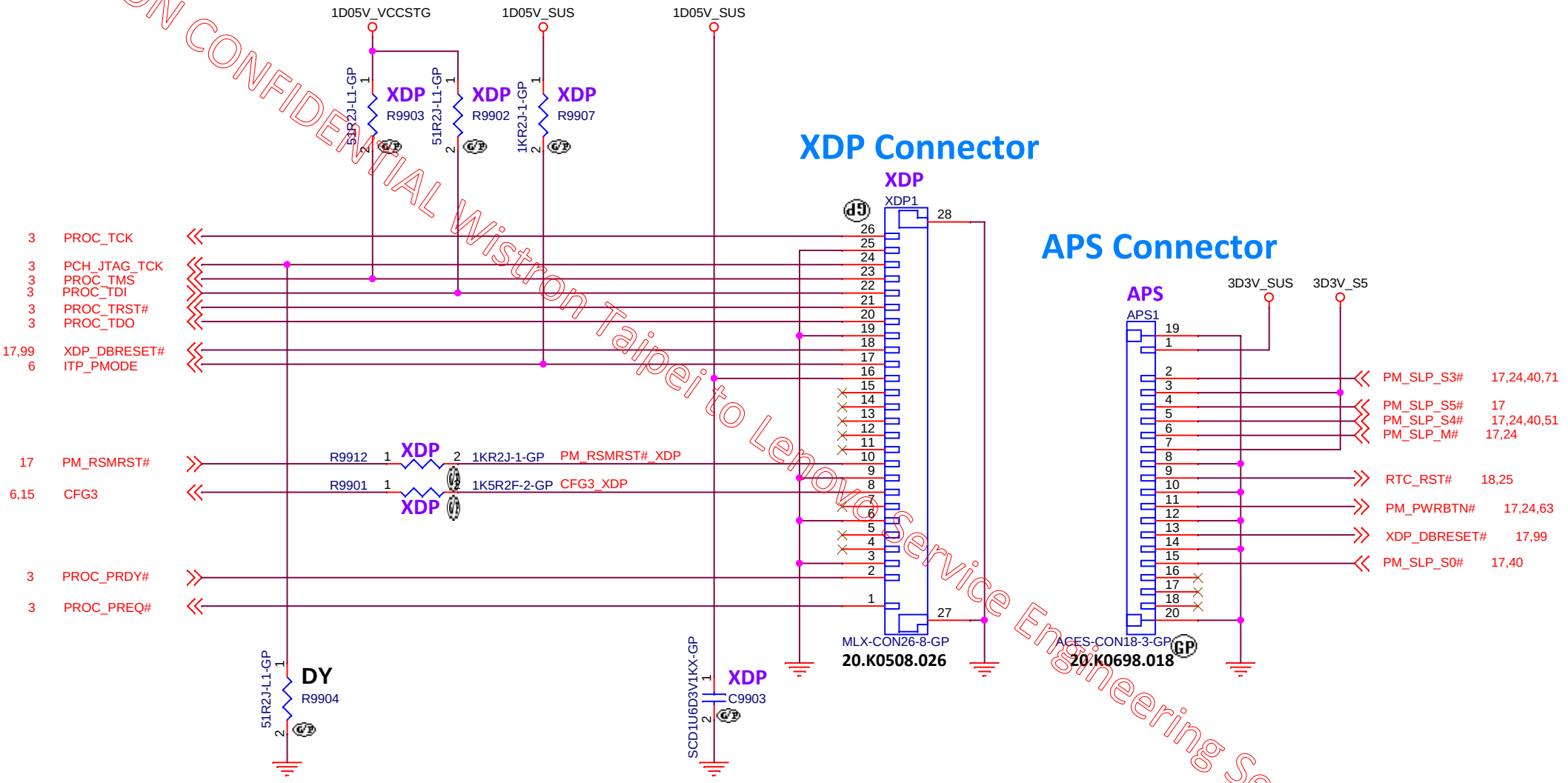
Main Func = Debug

BB1_EVT_MAIN_W021
BB1_EVT_MAIN_W032
BB1_FVT_MAIN_W017



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Title: ***DEBUG (XDP/APS)***

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